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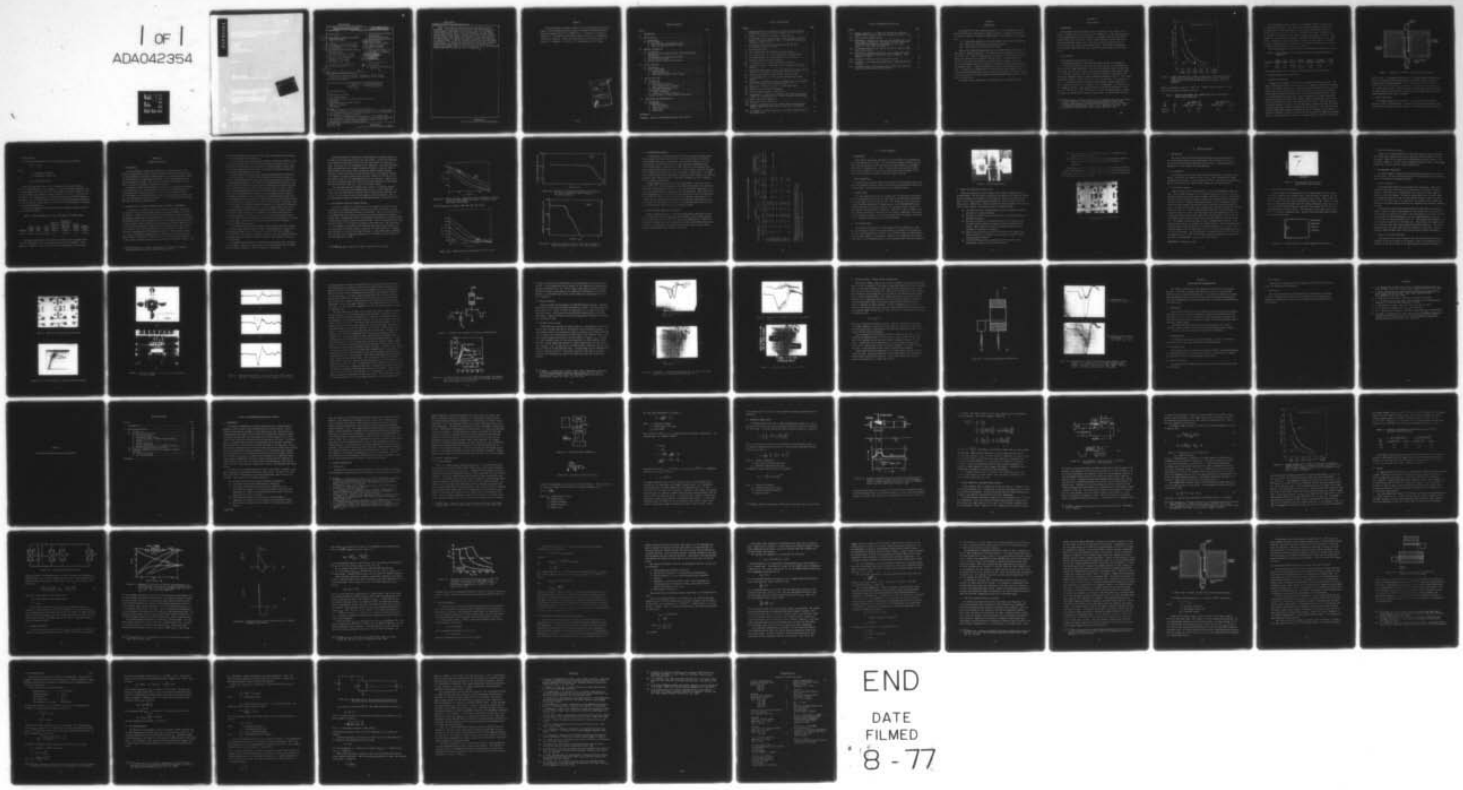

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The objectives of this research program are (i) to develop planar GaAs transferred-electron logic devices (TELDs) and (ii) to fabricate and evaluate a four-bit correlator.

The major accomplishments in this phase of the program were (i) significant progress in the advancement of basic device technology; (ii) the use of active devices as nonlinear loads; and (iii) the fabrication of critical building blocks.

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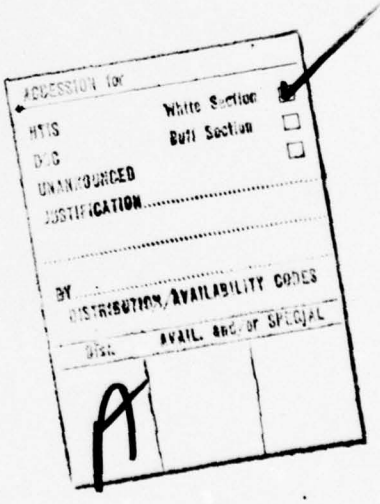
TELDs of the improved design type have been fabricated and evaluated. The previously used electrolytic thinning technique has been extended to GaAs wafers of the n^+-n-n^- type. The n^+ capping layers provide better ohmic contacts to the device and thus reduce the threshold voltage values. A capacitive pickoff output electrode has been added to the standard TELD structure. This new structure eliminates some of the memory and stability problems associated with the standard TELDs. A two-bit correlator circuit has been fabricated and evaluated. To improve the compatability of TELD input and output signal levels, active (FET) devices have been used as either load resistors or trigger elements. Pulses as small as 150 ps were processed through TELD-FET inverters with a 2-4 voltage gain.

PREFACE

This Annual Report describes research done in the Microwave Technology Center of RCA Laboratories under Contract No. N00014-75-C-0100 during the period 15 December 1975 to 14 December 1976. F. Sterzer is the Center's Director; S. Y. Narayan was the Project Supervisor, and L. C. Upadhyayula the Project Scientist. Others who participated in the research are R. E. Smith, J. F. Wilhelm, S. T. Jolly, J. P. Paczkowski, and J. E. Brown.



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INTRODUCTION

The objectives of this research program are: (i) to develop planar GaAs transferred-electron logic devices (TELDs) and (ii) to fabricate and evaluate a four-bit correlator. The major accomplishments in this phase of the program were:

(i) significant progress in the advancement of basic device technology;

(ii) the use of active devices as nonlinear loads;

(iii) fabrication of critical building blocks.

TELDs of the improved design type have been fabricated and evaluated. The electrolytic thinning technique of GaAs wafers has been extended to wafers of the n^+-n-n^- type. The n^+ capping layers provide better ohmic contacts to the device and thus reduce the threshold voltage values. A capacitive pickoff output electrode has been added to the standard TELD structure. This new structure eliminates some of the memory and stability problems associated with the standard TELDs. A two-bit correlator circuit has been fabricated and evaluated. To improve the compatibility of TELD input and output signal levels, active (FET) devices have been used as either load resistors or trigger elements. Pulses as small as 150 ps were processed through TELD-FET inverters with voltage gain of two to four.

The effort in all these areas is described in the following sections.

SECTION II

DEVICE DESIGN

A. INTRODUCTION

New guidelines were developed in the first phase of this program for the design of transferred-electron logic devices (TELDs) [1]. These procedures were used in designing TELDs for this phase of the program. Mause has used three terminal TELDs with a capacitive pickoff output electrode in the 2-GHz multiplexer/demultiplexer circuit [2]. This device structure provides certain advantages over the regular (conventional) TELDs. The design considerations for the regular TELDs and TELDs with capacitive pickoff output are discussed below.

B. DEVICE DESIGN

1. Three-Terminal (Conventional) TELDs

A complete discussion of three terminal TELDs was given by Upadhyayula [1]. The critical parameters that were taken into account in this design procedure are (i) trigger sensitivity; (ii) RC time constants and device low-field resistance; and (iii) percentage current drop and available output signal amplitude. Material parameters and device geometry of TELDs for this phase of the program are selected using the design procedures described in Ref. 1. The trigger sensitivity curve for a gate reverse bias of 2.0 V from Ref. 1 is reproduced in Fig. 1. A desirable value for minimum trigger voltage (trigger sensitivity) ΔVg is between 0.5 and 1.5 V. From Fig. 1, this corresponds to a channel pinch-off voltage of 22-50 V. From domain dynamics it has been established [3] that $nd \geq 10^{12}$ cm^{-2} and $nl \geq 10^{13}$ cm^{-2} where n, d, and l are doping density, channel thickness, and device transit length, respectively. For good current dropback,

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1. L. C. Upadhyayula, "Trigger Sensitivity of Transferred Electron Logic Devices (TELDs)," IEEE Trans. Electron Devices ED-23, 1049-1052 (Sept. 1976).
2. K. Mause, "Multiplexing and Demultiplexing Techniques with Gunn Devices in the Gigabit-Per-Second Range," IEEE. Trans., MTT-24(12), 926 (Dec. 1976).
3. K. Heime and A Schlachetzki, Electron. Lett. 8(8), 203 (1972).

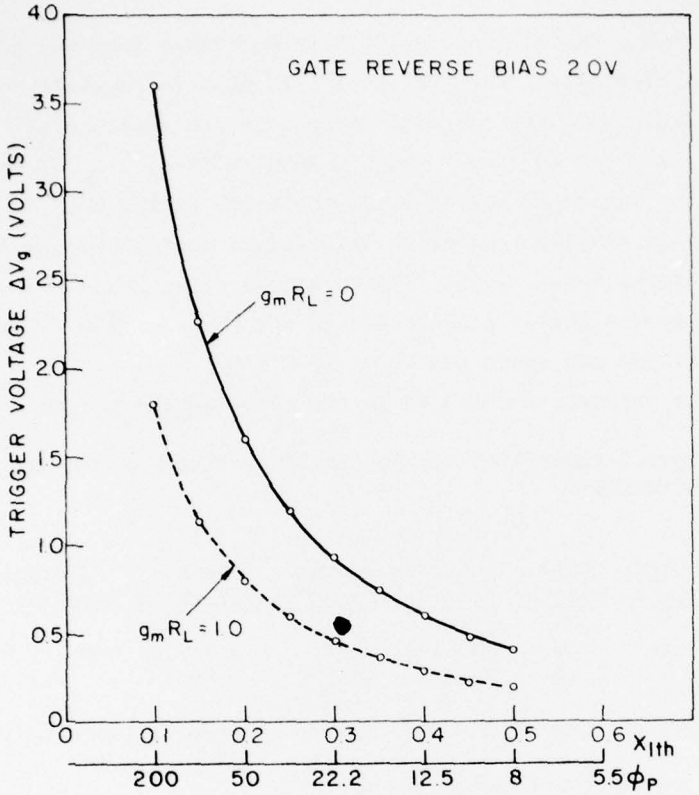


Figure 1. Trigger sensitivity of a TELD as a function of fractional depletion width (x_{1th}) or pinch-off voltage ($\phi\rho$) for ϕ = 2.0 V. nd is kept constant and both n and d are allowed to vary; g_mR_L is used as a parameter.

however, nd should be about 2-4 x 10^{12} cm^{-2}. Table 1 lists the material parameters that will meet the design criteria.

TABLE 1. MATERIAL REQUIREMENTS FOR CONVENTIONAL TELDs AS PER OUR NEW DEVICE DESIGN GUIDELINES

ΔV_g (V)	$\phi\rho$ (V)	nd = 2×10^{12} cm^{-2}		nd = 4×10^{12} cm^{-2}	
		n ($\times10^{16}$ cm^{-3})	d (μm)	n ($\times10^{16}$ cm^{-3})	d (μm)
0.5-1.0	22	1.3	1.54	5.2	0.77
0.8-1.6	50	0.6	3.5	2.9	1.75

A load resistance value of 50-100 Ω is desirable from the point of view of the RC time constants. A g_m value of 5-10 mmho is required to maintain $g_m R_L \simeq 0.25$ to 1.0. When the material parameters are selected so that $nd \simeq 2 \times 10^{12}$ cm^{-2}, $n \simeq 2 \times 10^{16}$ cm^{-3} and $\mu \simeq 5000$ cm^2/V-s, a g_m of 5-10 mmho can be realized in a device with gate width-to-length ratio, W/l_g, of 50-100. Gate length of 2 μm is readily realizable by standard photolithographic device fabrication. Therefore, a gate width (device width) of at least 100 μm is required. In order to keep the device dissipation in the range of 100-150 mW, the spacing between the cathode and anode has to be 12-15 μm.

The device parameters obtained in the above design are summarized in Table 2.

TABLE 2. DEVICE PARAMETERS FOR CONVENTIONAL TELDs AS PER OUR NEW DESIGN GUIDELINES

Parameter*	Device Length	Gate Length	Device Width	Doping Density	Channel Thickness	Trigger Sensitivity	Voltage Gain
Value	12-15 (μm)	2.0 (μm)	100-150 (μm)	1-2 ($\times 10^{16}$ cm^{-3})	0.7-2.0 (μm)	0.5-1.5 (V)	1-1.25

*Percentage current drop of 20-30% has been assumed in these calculations.

2. TELD with Capacitive Pickoff Output

a. Principle of Operation

Figure 2 is a schematic of a TELD with a capacitive output electrode. The anode, cathode, and Schottky gate construction is similar to that of the standard TELDs. The pickoff electrode is a narrow metal stripe isolated from the device's active region by a thin dielectric layer of SiO_2 or SiO or Al_2O_3. The TELD is biased below threshold, and domains are nucleated by applying a negative signal to the Schottky-barrier input gate. When the domain is in transit between the gate and the output electrode, the potential under the capacitive pickoff electrode increases and a positive pulse appears at the output. When the domain is in transit between the output electrode and anode, the potential under the output electrode drops and a negative pulse appears at the output. The capacitive pickoff probe essentially samples the domain voltage as the domain passes under it. Either the positive or negative output pulse can be used for triggering succeeding stages. The device delay is equal to the domain formation time when the positive

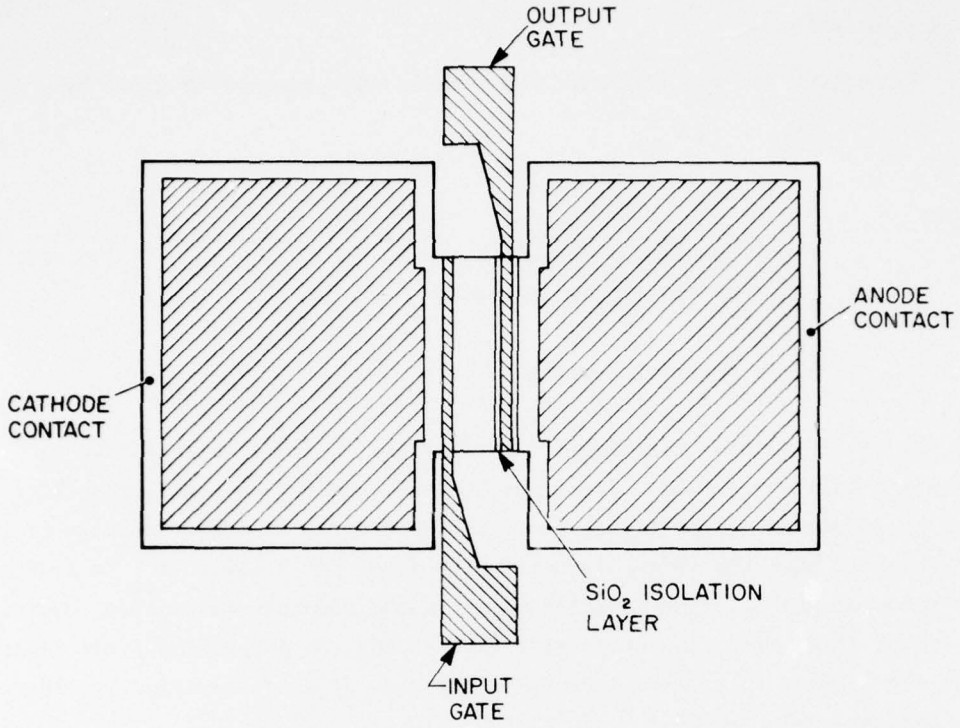


Figure 2. Schematic of TELD with capacitive pickoff output.

pulse is used. A throughput delay equal to the domain transit time from input gate to the output electrode results when the negative pulses are used for triggering the succeeding stages; *but, the maximum frequency at which these circuits work is still given by the transit-time frequency corresponding to the cathode-anode spacing.* Since the output is taken neither from the cathode nor anode, memory action will not take place in this device and true, stable single-domain operation will be possible.

b. Trigger Sensitivity

The trigger sensitivity of TELDs with capacitive output electrode is similar to that of standard TELDs. Therefore, the design considerations discussed in the previous section are valid also for TELDs with capactive output.

c. Output Voltage

The output voltage amplitude for a capacitive pickoff is given by

$$\Delta V_o = \alpha K V_{th}$$

where

α = coupling coefficient

K = percentage current drop

and

V_{th} = threshold voltage

Mause [2] pointed out that α is of the order of 0.75 when a TELD is driving a split-gate TELD. Even though K = 0.5 is theoretically possible, the best experimental values lie in the 0.3-0.35 range. An output voltage of 1-1.5 V is generated when the threshold voltage is about 5-7 V (i.e., ℓ_{ca} is 15-20 μm). The value of the coupling coefficient decreases when the capacitive loading is increased (i.e., for fan-out greater than 1) and the output amplitude decreases. This can be made up to some extent (at the cost of dc dissipation) by increasing the cathode-anode length ℓ_{ca}.

The device parameters selected for TELDs with capacitive output electrode are summarized in Table 3.

TABLE 3. DEVICE PARAMETERS FOR TELD WITH CAPACITIVE PICKUP OUTPUT

Parameter	Device Length (μm)	Gate Length (μm)	Device Width (μm)	Width of Capacitive Output Electrode (μm)	Dielectric Film Thickness for Capacitive Electrode (μm)	Doping Density ($\times 10^{16}$ cm^{-3})	Channel Thickness (μm)
Value	15-20	1.2-2.0	80-100	2-2.5	0.2-0.3	1-2	0.7-2.0

The design considerations for TELDs were reviewed, and new design guidelines were developed. They are described in detail in the appendix. This appendix is complete by itself and can be read independently of this report.

SECTION III

MATERIAL PREPARATION

A. INTRODUCTION

Our major emphasis on materials technology for TELDs has been on the growth of high-quality n-layers on semi-insulating (SI) GaAs substrates using the $Ga/AsH_3/HCl/H_2$ vapor phase epitaxial system. We have also recently begun the investigation of S implantation into both SI GaAs and high-resistivity epi-layers grown on SI GaAs. This section describes our materials research effort relevant to the goals of the present program.

The details of RCA's vapor hydride technique are well known and described in the literature [4]. The key goals of our materials research relevant to this program are (i) epitaxial growth of high-resistivity buffer layers, (ii) improvement of electron mobility in thin n-layers grown on SI substrates, and (iii) improvement of doping uniformity across relatively large area wafers. The first two goals are interrelated.

B. HIGH-RESISTIVITY EPITAXIAL BUFFER LAYERS AND MOBILITY IMPROVEMENT

An important prerequisite for the development of TELD MSI technology is the growth of thin (1-3 μm) n-layers with high electron mobility on SI GaAs substrates. A major problem in meeting this requirement is that the quality of bulk-grown Cr-doped SI GaAs substrates is not very good and is very variable. The problems with SI GaAs substrates include poor crystal perfection, high dislocation density, and Cr precipitates and inclusions. The poor quality of the SI GaAs substrate manifests itself as low electron mobility in thin n-layers grown thereon. The n-SI GaAs interface has a large number of traps. One method of compensating for the deleterious effects of poor substrate quality is to grow an epitaxial high-resistivity buffer layer. The quality of epitaxial layers, in general, is superior to that of the bulk-grown substrate. n-Layers grown on buffer layers have potentially higher electron mobility. The

4. J. J. Tietjen et al., "Vapor Phase Growth of Several III-V Compound Semiconductors," Solid State Technology 10, 42 (1972).

concept of epitaxial buffer layers is well known in semiconductor technology, and its utility has been established.

We are currently investigating three methods of epitaxial growth of high-resistivity layers. These are (i) chromium doping with CrO_2Cl_2 used as the doping gas, (ii) doping by the introduction of minute amounts of water vapor into the gas stream, and (iii) the use of controlled "background: doping by the judicious adjustment of gas flows.

Chromium doping with CrO_2Cl_2 has produced excellent-quality high-resistivity layers with $\rho > 10^7$ Ω-cm. TELDs fabricated from n-layers grown on epitaxial chrome-doped buffer layers have shown current drops as high as 28%. An independent assessment of the quality of chromium-doped epi-layers is provided by the fact that 1.5-μm gate GaAs FETs fabricated from wafers with such buffer layers operated at 22 GHz with output power close to 150 mW. Photoconductivity measurements carried out by the Electronics Research Branch of AFAL show that chrome-doped epi-layers had a much sharper Cr peak than the bulk-grown SI substrate. This is indicative of superior crystal perfection. The disadvantages of chrome doping are that CrO_2Cl_2 attacks the quartz reactor, and hence BN liners and sapphire feed tubes have to be used. Furthermore, the reproducibility of the chromium-doping process has to be improved considerably.

In a series of experiments, one of the gas streams going to the reactor was passed through a vessel containing water absorbed in an inert material. This vessel can be cooled to a low temperature to produce controlled low water-vapor pressure in the gas stream. Our goal was to determine whether this would result in high-resistivity layers due to the incorporation of oxygen as a deep level. High-resistivity layers with point contact breakdown in excess of 1000 V were realized.

Several "water doped" high-resistivity layers grown at RCA were analyzed at the Electronics Research Branch of AFAL. These layers were p-type, had a resistivity of about 7-10 x 10^4 Ω-cm, $p = 2.5 \times 10^{11}$ cm^{-3} and μ_p (300K) $\sim$ 320 $cm^2 V^{-1}s^{-1}$. The acceptor activation energy was 0.49 eV. Photoluminescence measurements did not show any evidence of oxygen. The acceptor has not yet been identified.

This method for high-resistivity growth is operationally more convenient than Cr doping. However, n-layers grown on such buffer layers have not shown improved electron mobility. Further research is in progress.

The third method for the growth of high-resistivity epitaxial layers is to reduce the carrier gas-flow rate into the reactor. It has been found that this reduces the growth rate and the carrier concentration for growth on SI GaAs. The reason for this phenomenon is not understood. The high-resistivity layers produced have point contact breakdown voltages in excess of 1600 V. Thin n-layers grown on such buffer layers have shown excellent electron mobility. Figures 3(a) and 3(b) show mobility-carrier concentration results for a number of recently grown wafers with thin n-layers at 300 and 77K, respectively. Note that the compensation factors are excellent. Figures 4(a) and 4(b) show doping profiles of two of these layers generated by the British Post Office Profiler (BPO) [5]. Note the excellent profile.

This technique has been developed only recently. Preliminary measurements on TELDs fabricated from wafers grown recently are just being made. If these TELDS show performance consistent with the measured Hall mobility, the utility of this method of buffer layer growth will be established. This is an operationally convenient method, and multilayer wafers can be grown *in situ*.

C. TWO-INCH-BORE HEAT-PIPE FURNACE REACTOR

In order to improve the uniformity across an epitaxial layer and develop a capability for handling substrate close to two inches in diameter, a large-bore reactor with heat-pipes furnaces was developed. The use of several sections of sodium-filled pipes allows very precise and uniform temperature profiles to be generated. The improved control of temperature uniformity has resulted in more uniform carrier density across an epitaxial wafer. This is particularly true when relatively thick ($\sim$ 5 μm) layers are grown on good substrates. For thin layers ($\sim$ 1 μm), however, the quality of the substrate also has a strong influence on the uniformity of the grown n-layer, since the n-SI GaAs interface is a significant fraction of the total epi-layer thickness. A good buffer-layer technology will therefore have a significant impact on the uniformity of thin n-layers of the type required for TELDs.

5. T. Ambridge and M. Faktor, Int. Phys. Conf. Ser. No. 24, 1975.

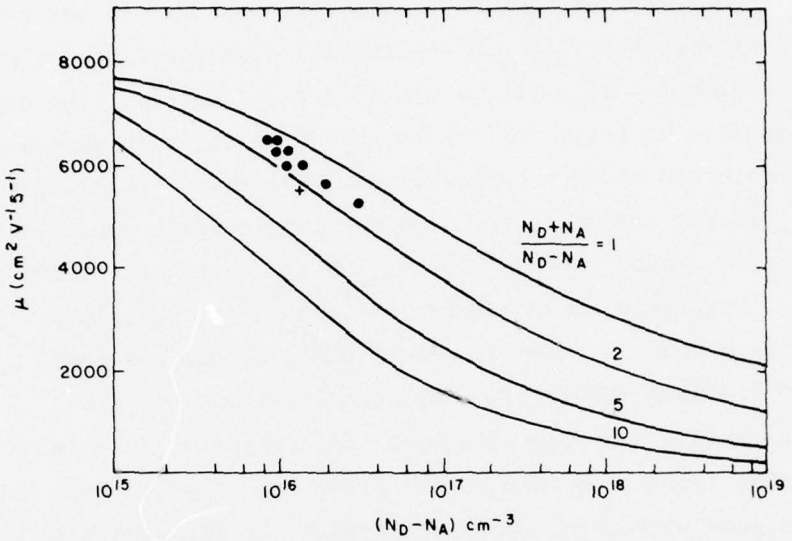


Figure 3(a). Mobility-carrier concentration results obtained at 300K on recent *thin* layers grown on SI GaAs. Theoretical curves also shown [6] for 300K.

6. D. L. Rode and S. Knight, Phys. Rev. B3, 2534 (1971).

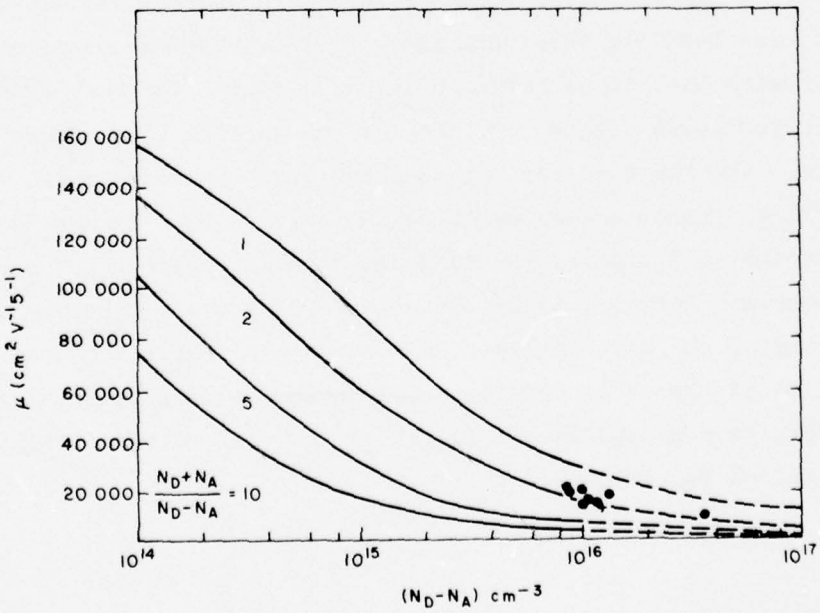


Figure 3(b). Mobility-carrier concentration results at 77K.

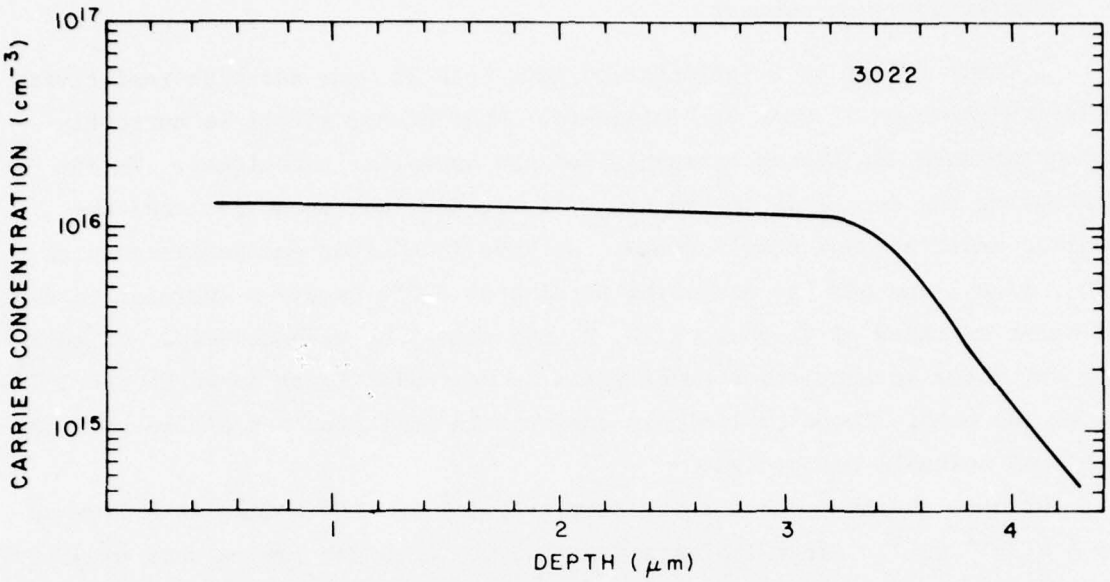


Figure 4(a). Profile of TELD epi-layer measured on BPO plotter. Note order of magnitude change in (N_D-N_A) in 0.6 μm at interface.

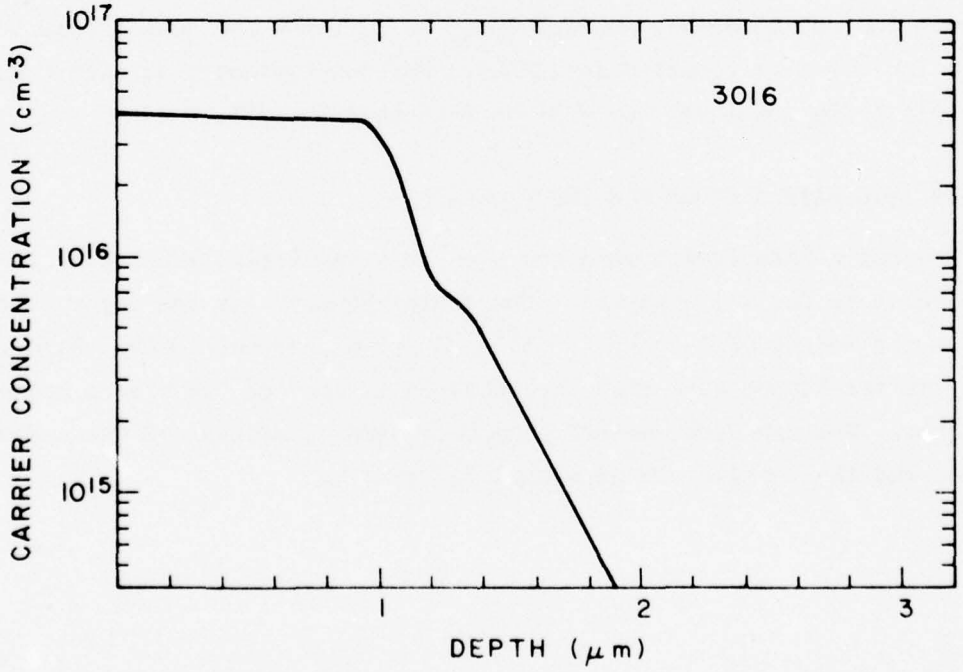


Figure 4(b). One micron epi-layer profile. Note order of magnitude change in (N_D-N_A) in less than 0.5 μm at interface.

D. ION-IMPLANTATION STUDIES

A small effort on S implantation into both SI GaAs and high-resistivity n-layers grown on SI GaAs was initiated. Most of our effort is currently being expended developing encapsulation and annealing techniques. We are evaluating the use of sputtered SiO_2, Si_3N_4, AlN, and unencapsulated annealing under arsenic overpressure. We have found that encapsulation with SiO_2, Si_3N_4, and AlN and annealing for 1 h at 800°C caused a decrease in doping at wafer surfaces of factors of 20, 2, and almost 0, respectively. In carrying out these encapsulation experiments an epitaxial layer doped in the 10^{16}-cm^{-3} range was used. These preliminary experiments indicate that AlN is perhaps the most suitable encapsulant.

We have obtained encouraging results using 230-keV S ions at a fluence of 4×10^{12} cm^{-2}. After implantation, 0.5-μm-thick AlN layers were reactively sputtered on and annealed at 825°C for 2 h. The relatively long anneal time was chosen in an attempt to obtain some drive-in diffusion. After anneal, the surface breakdown was in the 16-30-V range, indicating a carrier concentration in the 10^{16}-cm^{-3} range. Further evaluation is underway. Our plans are to evaluate the use of doubly ionized S and to increase the anneal time so as to obtain the 1.5-2 μm required for TELDs. Our ion-implantation effort has been at a relatively low level and will be increased in 1977.

E. SPECIFIC WAFERS GROWN FOR THE PROGRAM

Several n-GaAs layers were grown on semi-insulating substrates in both A and B reactors for this program. The doping density and the layer thickness were in the ranges of $1\text{-}3 \times 10^{16}$ cm^{-3} and 2-3 μm, respectively. High-resistivity buffer layers were also incorporated in some of the wafers grown in the A reactor. Van der Pauw measurements were made on several of these device wafers, and the results are presented in Table 4.

TABLE 4. VAN DER PAUW DATA FOR DEVICE WAFERS

Wafer	Growth Parameters		As-Grown Wafer				After Electrolytic Etching				After Electrolytic Etching with Photostimulation			
			300K		77K		300K		77K		300K		77K	
#	N ($\times 10^{16}$ cm^{-3})	d (μm)	n ($\times 10^{16}$ cm^{-3})	μ (cm^2/V-s)	n ($\times 10^{16}$ cm^{-3})	μ (cm^2/V-s)	n ($\times 10^{16}$ cm^{-3})	μ (cm^2/V-s)	n ($\times 10^{16}$ cm^{-3})	μ (cm^2/V-s)	n ($\times 10^{16}$ cm^{-3})	μ (cm^2/V-s)	n ($\times 10^{16}$ cm^{-3})	μ (cm^2/V-s)
B-240	1.2	5	2.4	5,460	2.0	12,760								
2438	1.5	3	5.0	3,530	4.1	8,220								
2568-A	1.5	2.5	1.2	7,230	1.1	16,390	1.6	7,230	1.52	16,390				
2568-B	1.5	2.5	1.0	6,510	0.96	17,100	0.76	6,200	0.71	18,000	0.51	5,880	0.51	16,760
B-268 (3-μ buffer)	2.0	3.0	2.8	5,480	2.25	13,100	2.4	4,500	1.8	13,000				
B-269	1 to 2	3.0	3.4	5,300	2.66	7,910								
B-270			2.27	5,610	1.8	13,000	2.2	5,100	2.0	11,800				
B-339*		1.0	6.4	3,900	5.2	5,700	-	-	-	-	-	-	-	-
B-340*		1.0	4.4	4,000	3.9	5,500	-	-	-	-	-	-	-	-
B-405	2.0	3.0	1.7	5,600	1.3	15,000	1.9	4,800	1.6	11,000				
B-412	2.0	3.0	2.2	5,700	1.8	14,000	2.2	5,600	1.8	15,000				

*B-339 and B-340 were etched electrolytically under photostimulation; estimated final thicknesses are 0.6 and 0.45 μm, respectively. No van der Pauw measurements were possible.

NOTE: Wafers #B-268 to B-412 were grown after heat pipes had been installed. Wafer #B-412 was anodically etched to voltage.

7. W. C. Niehaus and B. Schwartz, Solid-State Electronics 19, 175-180 (1976).

IV. DEVICE TECHNOLOGY

A. INTRODUCTION

Planar device technology developed in the first phase of the program was used in the fabrication of TELDs. The electrolytic-etching technique used to obtain uniform nd-product across the wafers has been modified to accommodate wafers with n^+ capping layers. The n^+ capping layers provide better ohmic contacts for the device. A new process schedule has been developed for the fabrication of TELDs with capacitive pickoff output electrode.

B. DEVICE FABRICATION

Standard (12-μm channel) TELDs, short-channel (3-4-μm channel) TELDs, and TELDs with capacitive pickoff output electrode have been fabricated during this program period. The fabrication procedures are described below.

1. Standard TELDs

With one exception, the process schedule for the fabrication of standard TELDs is essentially the same as that described in the "Microwave Shift Register" Annual Report dated 12 February 1976. The exception is the electrolytic etching of wafers containing n^+ capping layers. Al of 3000-4000-Å thickness is evaporated onto the n^+ capping layers, and the ohmic contact regions are delineated by photolithographic techniques. After Al is used as a mask on the ohmic regions, the wafer is electrolytically etched to completion; this establishes a uniform nd-product in the active regions across the wafer. The wafer is then processed as described in the above reference.

2. Short-Channel TELDs

The fabrication procedure for short-channel TELDs is identical to that for 12-μm devices. We used the existing mask sets intended for 2-μm-gate FET devices. Self-aligning-gate technology is not exactly suited for TELD fabrication, and this created a few problems. However, 3-4 μm TELDs have been fabricated; Fig. 5 is a photomicrograph of a short-channel device that was fabricated.

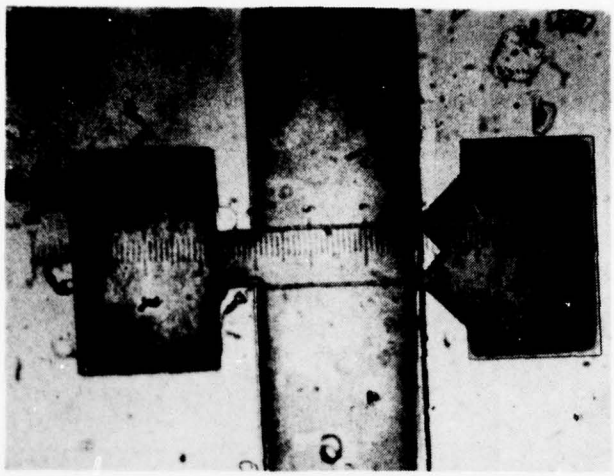


Figure 5. Short-channel device.

3. TELDs with Capacitive Pickoff Output

TELDs with capacitive pickoff output offer several advantages over the standard TELDs: (i) the output voltage does not depend on the absolute current drop in the device but depends on the percentage current drop only, and (ii) there is no RC time constant appearing across the device to keep it in the memory state. Therefore, a process schedule has been developed for the fabrication of these devices. The process steps are summarized below.

(a) The $\{0\bar{1}1\}$ and $\{011\}$ crystallographic planes are defined by means of preferential etching techniques.

(b) The wafer is electrolytically etched until a uniform nd-product is obtained throughout.

(c) The device structure is oriented along the $\{011\}$ direction, and the ohmic contact regions are opened by photolithographic techniques. Ohmic contacts are made by evaporating AuGe/Ni/Au and sintering at 380-400°C in hydrogen.

(d) Ohmic contact and active regions of the devices are masked, and devices isolated by etching in an anisotropic etch down to semi-insulating GaAs substrate.

(e) A 2000-3000-Å thick SiO_2 is deposited by CVD (chemical vapor deposition) technique at 325°C and densified.

(f) A 2.5-μm-long SiO_2 film is defined closer to the anode for the capacitive-output electrode.

(g) The input Schottky-barrier gate and capacitive-output electrode regions are opened, and Cr/Au of 1500-2000-Å thickness is evaporated.

Provision was made to interconnect groups of three devices to perform a two-input AND/CORRELATION. The devices were diced and separated for further evaluation. Figure 6 shows a photomicrograph of a fabricated 20-μm-channel TELD with capacitive pickoff output.

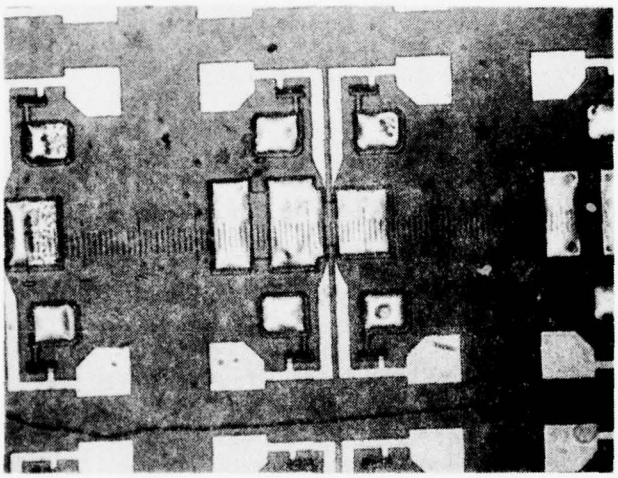


Figure 6. 20-μm-channel TELD with capacitive pickoff output.

V. DEVICE EVALUATION

A. INTRODUCTION

The three device structures fabricated during this program period are (i) 12-μm channel devices, (ii) short-channel (2-4 μm) devices, and (iii) 20-μm channel devices with capacitive pickoff output. High-frequency and dc parameters of these devices have been measured.

B. dc EVALUATION

The threshold current and current drop were measured on a Tetronix* curve tracer. The device was biased at about 0.95 V_{th}, and a negative-step signal was applied at the gate. A series resistance of 140 Ω was used in these measurements (the sensitivity of TELDs strongly depends on the load resistor).

1. 12-μm-Channel Devices

Figure 7 shows the I-V characteristic of a 12-μm cathode-anode channel device. The threshold voltage is 7.0 V; threshold current is 70.0 mA. The percentage current drop is 21.0, and the trigger sensitivity is 1.0 V. It has been observed that the threshold voltage is always 2-3 V higher than the theoretical value of 4.2-4.8 V. Computer simulations carried out on a concurrent program showed that high fields exist near the anode on devices with planar ohmic contacts. In order to circumvent this problem, ohmic contacts were made into etched holes of 0.1-0.2 μm. There is some indication that the threshold voltage decreased by 0.5-1.0 V, but it was still higher than the theoretical value. The percentage current drop was much smaller than the theoretical value of 50% and considerably smaller than the best results (30-40%) reported in the literature [2]. The smaller current drop might be due to somewhat poorer quality of the material and/or due to the presence of trapping centers. The best trigger sensitivity measured is about 0.8-0.9 V; the typical value is 1.2 V. This is considerably higher than the design goal of 0.5 V. The poor sensitivity may be due to one of two factors: (a) the nd-product is larger ($3.5\text{-}4.2 \times 10^{12}$ cm^{-2}) than the desired value (2×10^{12} cm^{-2}) and (b) the electron mobility and hence the low-field transconductance (g_m) are lower than desired.

*Tetronix Inc., Beaverton, Oreg.

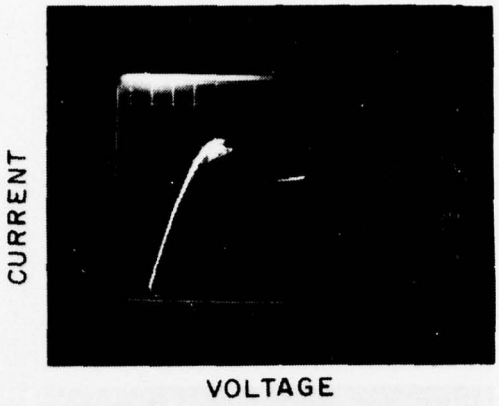


Figure 7. I-V characteristic of a 12-μm cathode-anode channel device.

2. Short-Channel (3-4 μm) Devices

Figure 8 shows the I-V characteristic of a short-channel (3-4 μm) device. This device exhibits a nice current drop. From the figure it appears that the threshold voltage is 1.0 V and the threshold current, 35 mA. The current drop-back is nearly 25-30%; the device dissipation is nearly 35 mW. Later, the high-frequency measurements indicated that the negative-resistance effect seen in the I-V characteristic may be associated only with low frequency but not with the transferred-electron (Gunn) effect. The nd-product in this wafer may be about 10^{12} cm^{-2}, which is a marginal value. Devices from other wafers showed smaller percentage current drop.

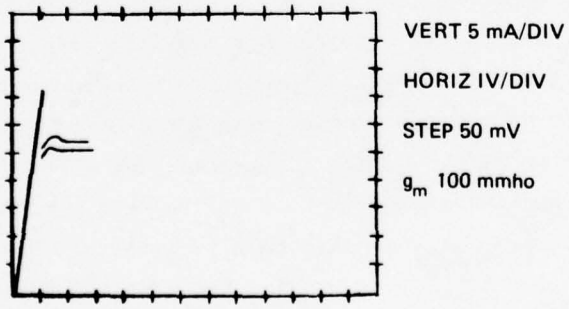


Figure 8. I-V characteristic of a short-channel (3-4 μm) device.

3. TELDs with Capacitive Output

Figure 9 is a photomicrograph of a TELD with capacitive output electrode. The cathode-anode spacing is 20 μm; the capacitive probe is spaced 5 μm from the anode. Figure 10 is a typical I-V characteristic of such a device. The threshold voltage is 7.5-8.0 V, and the threshold current is 40 mA. The trigger sensitivity is 1.0 V, and the current dropback 25%.

C. HIGH-FREQUENCY EVALUATION

The high-frequency evaluation of these devices was carried out in microstrip circuits. The test circuits used are (a) source followers, (b) inverters, and (c) coincidence or correlator circuits.

1. Two-Bit Correlator

Split(dual)-gate TELDs are very suitable for correlators. Three 35-μm TELDs with split gates were used in the fabrication of a two-bit correlator circuit. Figure 11(a) is a photograph of the circuit; Fig. 11(b) shows the details of the chip bonding. The two-bit inputs were fed to the split gates of two TELDs through 50-Ω lines, and the cathode outputs of these two TELDs were fed to the split gates of a third TELD. The output at the cathode load resistor of the third TELD was monitored on a sampling scope through a sampling resistor.

The correlator circuit was tested with pulse inputs from a charge-line pulser. Figure 12 shows the performance of the circuit with (i) one input in "1" state and the other in "0" state or (ii) both inputs in "1" state. The circuit appeared to work satisfactorily, but the trigger sensitivity was poor ($\tilde{\sim}$ 2.4 V) and the output was small ($\sim$ 0.3 V). This marginal performance is due to the earlier version of (35 μm) TELDs used. These devices were employed because they have split gates and integral cathode load resistors. Also, 12-μm channel devices with split gates were not available at that time. Recently developed improved TELDs (12-μm type) should result in better performance.

2. Inverters and Source Followers

TELD inverters and source followers with chip load resistors have been evaluated in the first phase of this program. Some of the problems that remained to be solved are those of (i) generating output signals comparable to

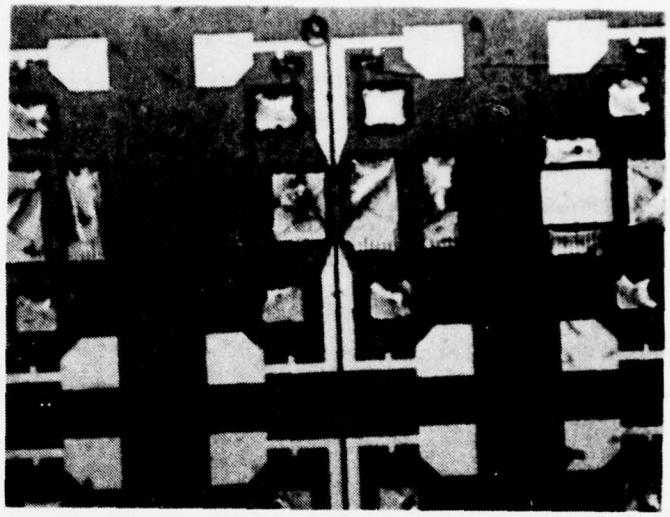


Figure 9. TELD with capacitive-output electrode.

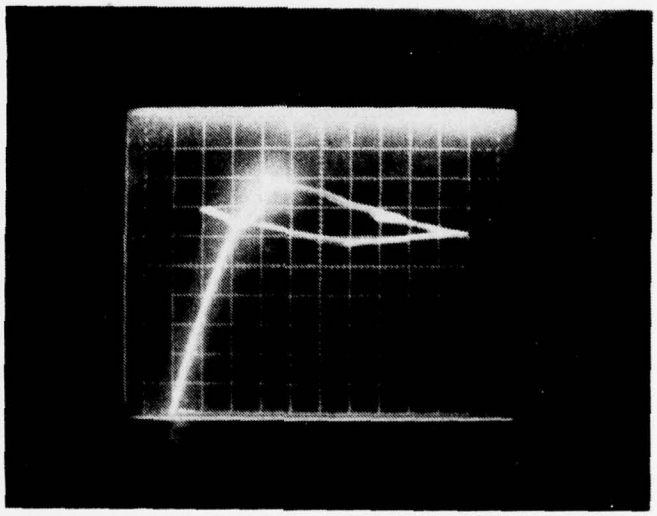
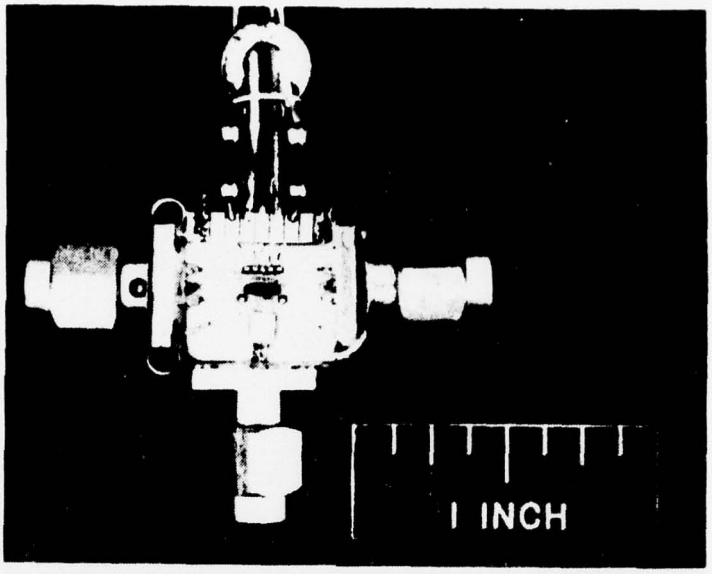
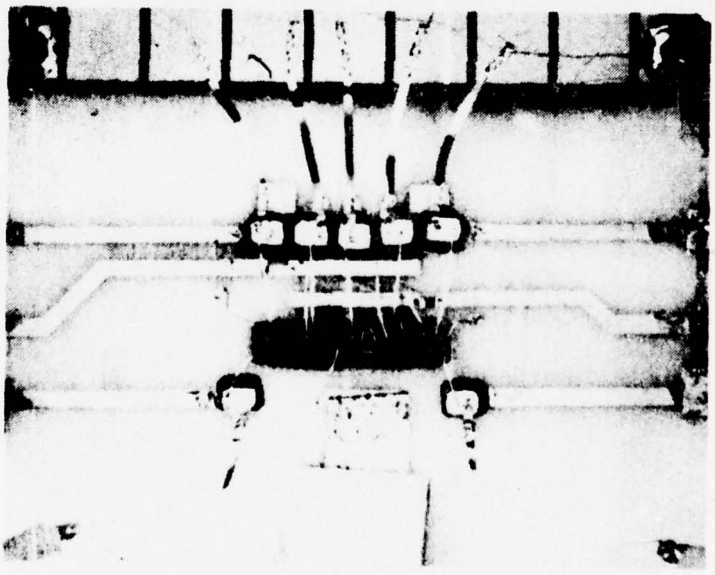


Figure 10. I-V characteristic of capacitive output electrode.

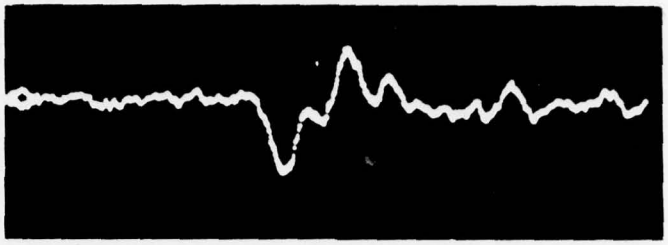


(a)

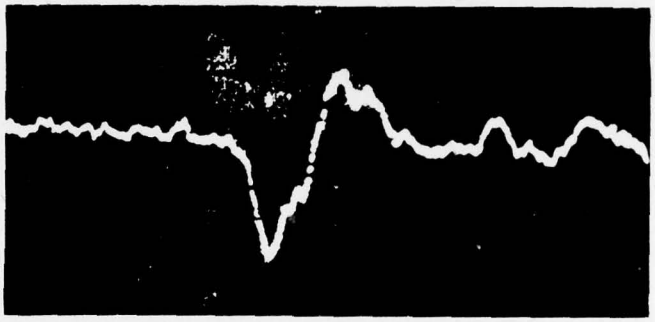


(b)

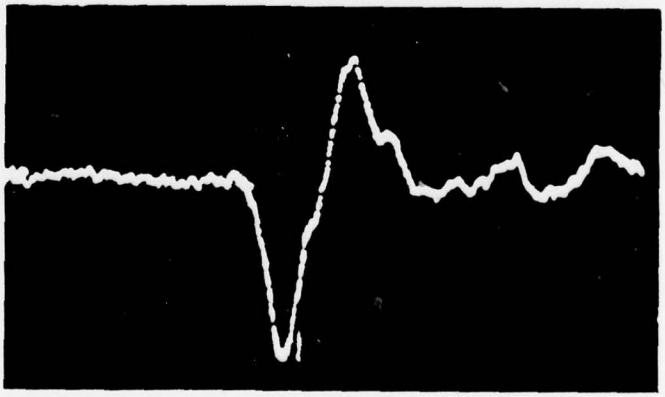
Figure 11. Two-bit correlator. (a) Circuit and (b) details of the chip bonding.



(a)



(b)



(c)

Figure 12. Correlator output with: (a), (b) one input in "1" state and the other in "0" state and (c) both inputs in the "1" state.

the inputs required without any deterioration in the high-frequency performance; (ii) maintaining the stability of the circuits against spurious triggering and memory action; and (iii) keeping the total dissipation low ($\sim$ 100-200 mW/gate). The use of active devices as nonlinear load resistors can eliminate problems (i) and (iii) above. We tried a few experiments with FETs as load resistors. As the TELD and FET were not fabricated on the same chip, it was rather difficult to match the currents in the two devices and operate both under optimum conditions. Also, the trigger sensitivity of the TELDs available at that time was 1.2-1.5 V. We, therefore, attempted to use FET as trigger element and TELD as nonlinear load.

The transconductance of FETs is much larger than that of TELDs for similar device structures. We therefore studied pulse amplifier circuits with FET as trigger element and TELD as nonlinear load. Figure 13 is a TELD-FET inverter. The operation of this circuit can be explained with the help of the I-V characteristic shown in Fig. 14. The devices (FET and TELD) were chosen so that the drain current of the FET for zero gate-source voltage was higher than that of the peak (threshold) current for the TELD. A load line is drawn with a slope equal to the inverse of the low-field resistance of the TELD. The operating voltage for the TELD-FET combination was chosen so that when the circuit is triggered the voltage available for TELD would exceed the threshold value. The operating bias and the load line fix the quiescent biasing condition. To maintain the quiescent current, FET gate was returned to a negative supply voltage. Also, the bias point was selected so that the quiescent current would be below the peak current and above the valley current for TELD. A positive input applied to the gate of FET increases the drain current momentarily to a value above peak current of the TELD. The load line is such that the voltage across the TELD increases above the threshold value. Under these conditions high-field domains form in TELD, and the current drops. Since the valley current of the TELD is lower than the quiescent current, the operating point on the FET shifts into the linear part of the I-V curve. A substantial voltage change thus occurs at the drain of the FET, and a negative output pulse is produced with high voltage gain. The TELD-FET combination described above works as an inverter. In many applications the circuits have to be cascaded, i.e., the output of the first circuit must be capable of triggering the following circuit. This requires the output of the pulse amplifier to be of the same polarity as the input trigger pulse.

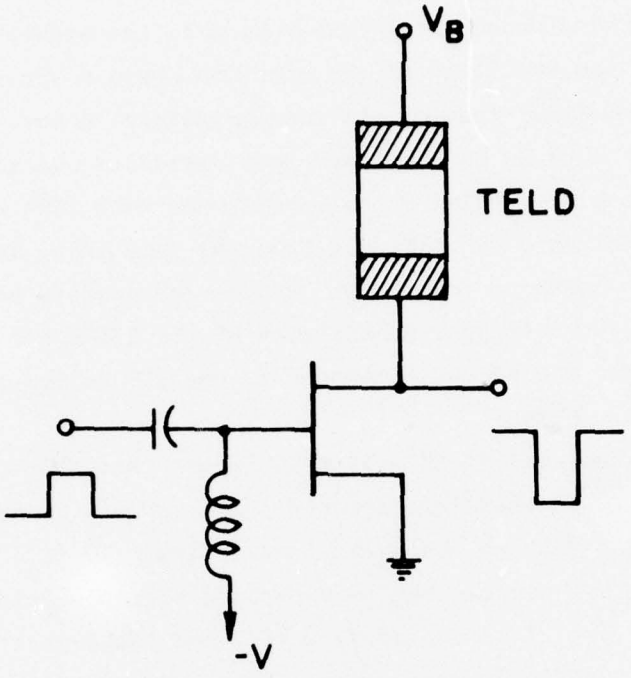


Figure 13. TELD-FET pulse amplifier with TELD as nonlinear load.

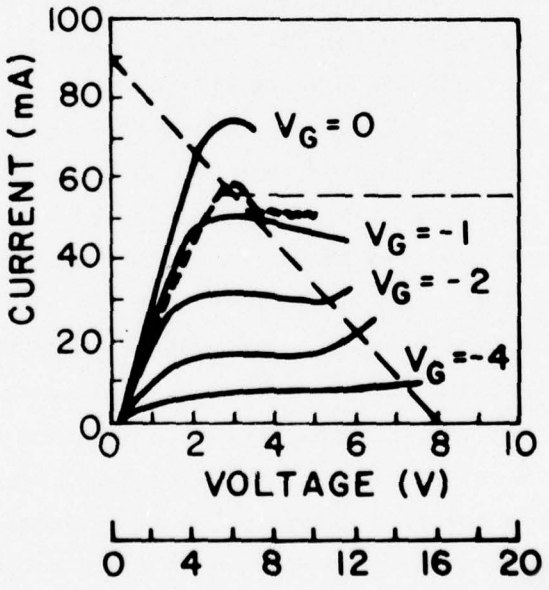


Figure 14. I-V characteristic of a FET with TELD characteristic superimposed. (The lower voltage scale (0-20) applies to the TELD; the current scale is the same for both devices.)

In order to achieve this the TELD has to be incorporated in the source side of the FET. This configuration will be similar to the common drain configuration discussed by Mause et al. [8]. When a linear load resistor is used, it is not possible to obtain voltage gain in the common drain configuration. The TELD, however, is a nonlinear load, and it can be shown that a voltage gain of up to 2.0 is possible.

a. TELD-FET Inverter

Figure 15 shows the performance of a TELD-FET inverter circuit. Pulses as narrow as 150 ps have been processed through this circuit. The pulse amplifier has a gain of 2-4. Figure 16 shows the performance of the same circuit for a wide input pulse. Near-transit-time oscillations characteristic of the TELD are present. These observations confirm the principle of operation of the circuit discussed earlier.

b. TELD-FET Source Follower

A TELD-FET source follower is shown in Fig. 17. The operation of this circuit is more critical than that of the inverter circuit discussed earlier. In the quiescent state it is necessary to match the current in the TELD and FET and also to maintain the voltage across the TELD close to the threshold value. The input trigger signal must produce a current change $\Delta I = g_m \Delta V_g = I_{th} - I_q$ where I_q is the standoff current and the other terms have the usual meaning. Also, the input trigger signal must produce a voltage change across the load equal to $\Delta V_g = g_m \Delta V_g R_o = V_{th} - V_q$ where R_o is the TELD low-field resistance and V_q is the voltage across it in the quiescent state. The performance of the TELD-FET source follower is shown in Fig. 17. The output polarity is the same as the input polarity; the voltage gain is unity; the output also shows the transit-time behavior.

8. K. Mause, A. Schlachetzki, E. Hesse, and H. Salow, "Monolithic Integration of Gallium Arsenide-Gunn Devices for Digital Circuits," Proc. Fourth Biennial Cornell Electrical Eng. Conf. Microwave Devices, Circuits and Applications, Ithaca, N.Y., Vol. 4, p. 211, 1973.

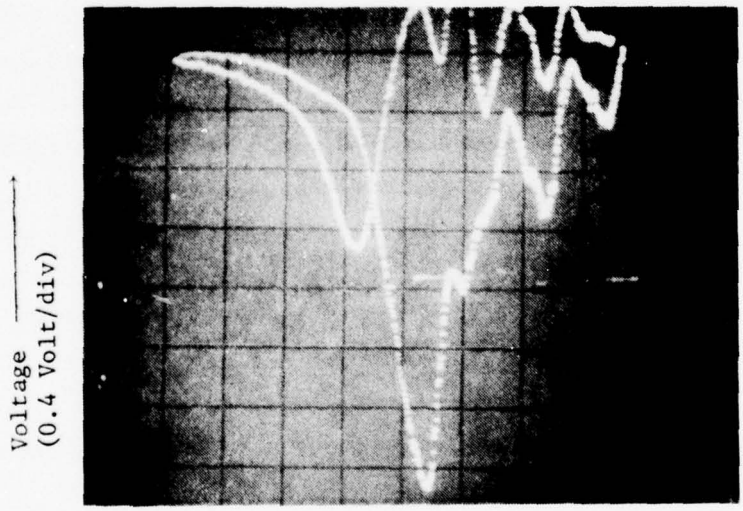


Figure 15. Performance of TELD-FET inverter when TELD is (a) in the linear part of I-V and (b) in the nonlinear part of I-V.

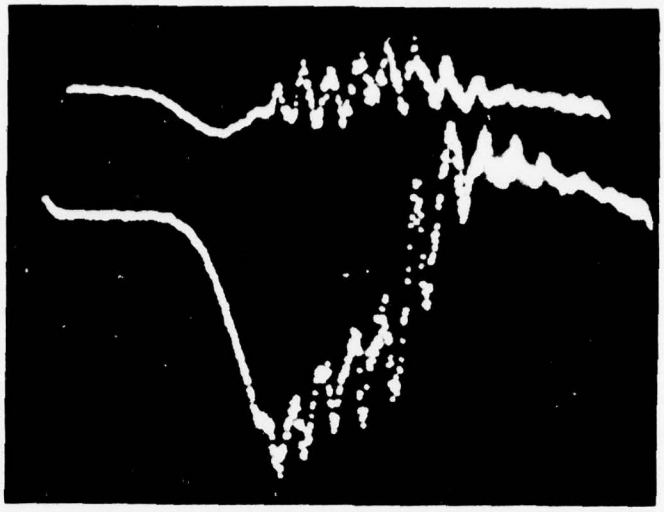


Figure 16. Response of a TELD-FET circuit to a wide input pulse.

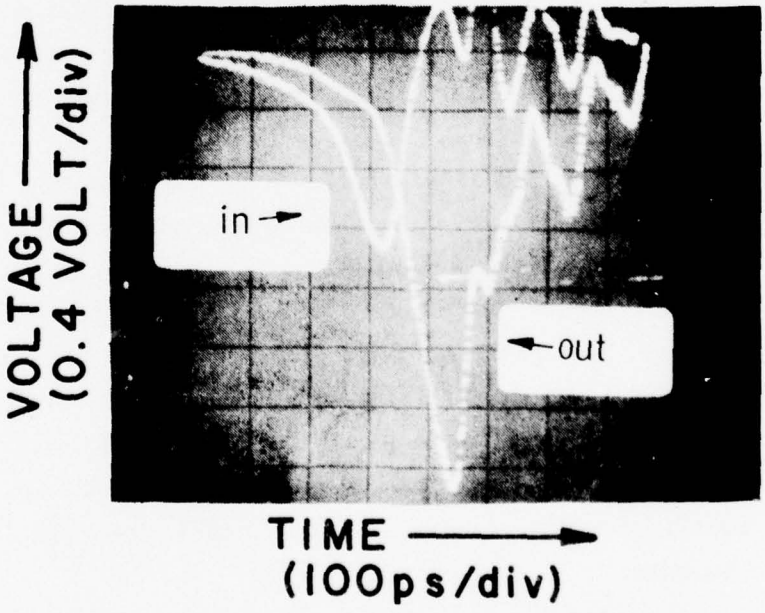


Figure 17. TELD-FET source follower performance.

D. BIASING OF TELDs - VIRTUAL GROUND CONFIGURATION

Basically, a TELD is used as (a) a source follower (to produce same polarity output) or (b) an inverter. The output is generated across an active or a passive load. In the source follower the load resistor is in the cathode side, and in the inverter it is in the anode side. When the load resistor is in the cathode side, because of the voltage drop in the resistor, the Schottky-barrier input-gate is heavily reverse biased. The trigger sensitivity is therefore reduced (see Ref. 1), the stability becomes poor, and the output amplitude decreases. A new biasing scheme called the virtual grounded-cathode configuration was found to eliminate the above problems. In this configuration the anode is returned to the positive bias (V_a), and the cathode through resistor R_K is returned to a negative supply voltage ($-V_K$) as shown in Fig. 18. The negative bias ($-V_K$) is selected so that

$$-V_K + R_K I_{th} = 0$$

where I_{th} is the device threshold current. When V_K is selected in this way, the cathode terminal is virtually at zero potential. The reverse bias on the Schottky-barrier gate is approximately the built-in voltage; this allows us to realize the best device performance.

The performance of a TELD source follower is shown in Fig. 19. A 12-μm cathode-anode spacing device from wafer B-91 was used. A 100-Ω resistor was used in the cathode, and the gate was returned to ground through a 50-Ω resistor. Figure 19(a) shows performance of the circuit with a single-bias scheme (i.e., cathode load resistor returned to ground). The output is small and noisy. No well-defined transit-time oscillations were observed.

Figure 19(b) shows the performance of the same circuit when the two-bias scheme was used. The output amplitude is more than doubled, and well-defined transit-time oscillations are present. This clearly shows that a two-bias scheme is far superior to a single-bias scheme.

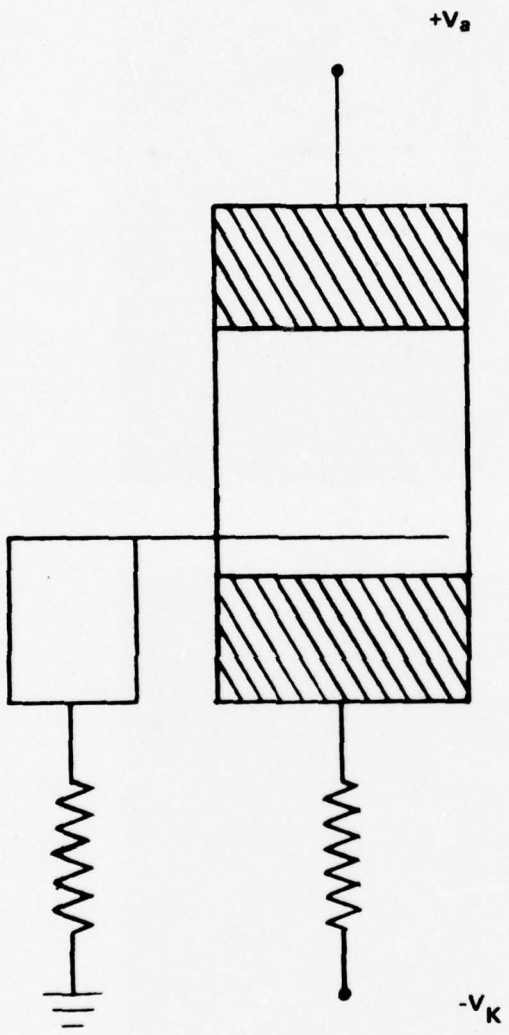
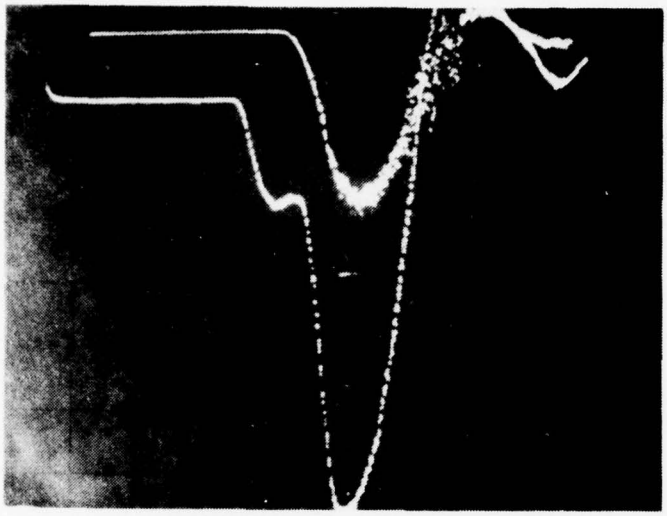
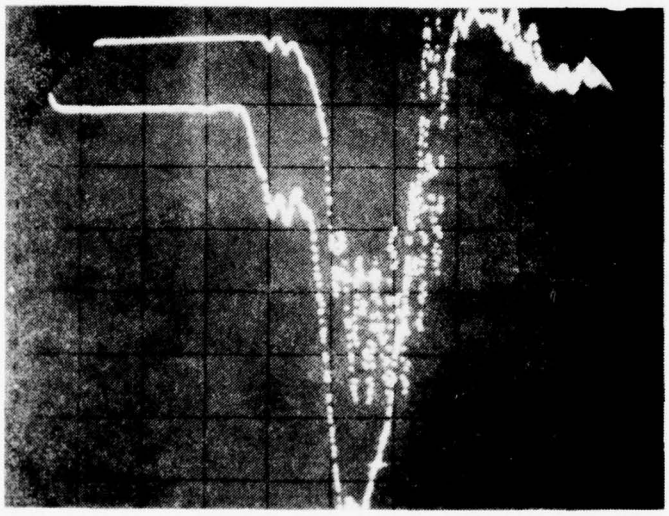


Figure 18. Virtual grounded-cathode configuration.



(a) Single-bias scheme:
V_a = 10.3 V, I_{th} = 52 mA



(b) Virtual grounded-cathode bias scheme: V_a = +6.0 V, V_K = -6.0 V, I_{th} = 62 mA

Figure 19. Performance of a TELD source follower under different biasing schemes: (a) single-bias and (b) virtual grounded-cathode scheme. Top trace: output; bottom trace: input. Vertical scale: 0.4 V/div; horizontal scale: 500 ps/div.

SECTION IV

CONCLUSIONS AND RECOMMENDATIONS

The results achieved under this program were presented in the previous sections. From this it appears that TELDs will find use in systems where speed is one of the major considerations. It is, however, necessary to evaluate these devices further before they can be used in subsystem applications. This section summarizes the results achieved thus far and makes recommendations for future work.

A. CONCLUSIONS

Devices were fabricated as per the improved design criteria and evaluated. The process for the electrolytic thinning of wafers was extended to use with the n^+-n-n^- type of wafers. A capacitive pickoff electrode was added to the TELD structure; this should eliminate the memory and stability problems associated with standard TELDs.

A TELD-FET combination was tested as both an inverter and a source follower. Pulses as small as 150 ps were processed through these circuits.

A two-bit correlator circuit was fabricated and evaluated.

B. RECOMMENDATIONS

The TELD-FET combination looks very promising. To make it a practical structure, further work must be done in the following areas:

1. Materials Growth

Modifications have to be made in the growth system so that semi-insulating or high-resistivity buffer layers can be grown on a routine basis to improve the electrical quality of thin epitaxial layers grown.

2. Device Fabrication

Integrated hybrid TELD-FET devices with capacitive output electrode must be fabricated.

3. Test Vehicles

Integrated test vehicles such as correlators and exclusive OR circuits have to be fabricated and evaluated.

4. Fabrication

The major effort must be directed toward the fabrication of monolithic circuits. Processes for producing passive elements such as resistors and capacitors, interconnects, crossovers, and multilevel metallization have to be developed.

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APPENDIX

DESIGN OF TRANSFERRED-ELECTRON LOGIC DEVICES

TABLE OF CONTENTS

DESIGN OF TRANSFERRED-ELECTRON LOGIC DEVICES*

1. INTRODUCTION

This write-up summarizes the design considerations for developing multigigabit-rate MSI circuits using transferred-electron logic devices. The two classes of GaAs devices suitable for multigigabit-rate logic applications are transferred-electron logic devices (TELDs) and field-effect transistors (FETs). We believe that GaAs FETs will find application in MIS circuits of up to about 5 Gb/s, while TELDs have the potential for operating up to 10 Gb/s. Our philosophy is to regard TELDs and FETs as complementary and not mutually exclusive. MSI circuits can be realized with both FETs and TELDs on the same chip. We will show that an integrated device with an FET input section and a TELD output section with a capacitive pickoff output electrode is the structure with most promise. The characteristics of this integrated structure are (a) good trigger sensitivity; (b) high voltage gain and hence fan-out capability; (c) compatible input/output levels, eliminating the need for level shifting; and (d) capability of stable operation under MSI constraints without self-triggering. With discrete FETs and TELDs we have obtained voltage gain of about 4 for operation with 100-ps pulses.

Our objective in pursuing programs on TELDs is to develop a flexible, viable MSI technology for multigigabit-rate logic applications. In view of this ultimate goal, we have concentrated on developing technology under realistic constraints. These include the following conditions:

(a) The input and output of logic gates should be compatible.
(b) Logic gates should remain stable while in operation.
(c) Logic gates should have fan-in and fan-out capability; i.e., they should be capable of driving the interconnect lines and input impedances of a number of succeeding logic gates without rise time degradation and loss of stability.
(d) Logic functions should be realized with a minimum number of components, to minimize power dissipation and interconnect delays.
(e) Device power dissipation must be minimized to obtain high packing density.

*Jan. 1977.

These constraints are interrelated and therefore require very careful trade-off analyses. The relaxation or ignoring of one or more of these constraints can lead to erroneous conclusions. This is one of the major reasons for the discrepancy between overoptimistic theoretical projections and the experimental results achieved to date. For example, based on power-dissipation considerations alone, an early publication estimated that an optimized TELD-load resistor combination will consume 25 mW, leading to a packing density of 100 gates/mm^2 [1]. If such devices were fabricated, however, they would have a resistance of 1 kΩ. Even for unity fan-out, the RC time constant due to this resistance and the input capacitance of the following gate will result in self-triggering and hence unstable operation. The situation will be further aggravated if higher fan-out is required. This condition holds even when interconnect capacitances are ignored, and therefore applies to closely spaced integrated logic circuits. This is just one example of the pitfalls of ignoring any one of the constraints. We will show that the use of an integrated TELD-FET structure makes it possible to meet all of these constraints and to develop a viable MSI technology.

2. DESIGN CONSIDERATIONS

2.1 Introduction

Transferred-electron logic devices (TELDs) have been designed, fabricated, and evaluated as single gates [2-4] and rudimentary integrated circuits [1,5,6].

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5. N. Hashizume and S. Kataoka, "Integration of GaAs MESFETs and Gunn Elements in a 4-Bit-Gate Device," Electron. Lett. 12(15), 370-372 (1976).
6. S. Yanagisawa, O. Wada, and H. Takahashi, "Gigabit Rate Gunn-Effect Shift Register," Tech. Digest, Int. Electron Device Meeting, Washington, D.C., 1975, p. 317.

Early theoretical calculations projected that logic gates with fan-out capability of between 6 and 10 are feasible [7]. Experimental results have not yet borne out these theoretical predictions. Voltage gains (and hence fan-out capability) of 0.5 for split-gate devices and one for single-gate devices have been demonstrated. The device dc dissipation in these experimental studies was, at best, 200-300 mW and approximately an equal amount of dc power was dissipated in the load resistor. This performance is clearly unacceptable for MSI logic circuits. We will now consider the critical design parameters and limiting factors of TELD logic circuits. We will discuss (a) RC time constants, (b) percentage current drop and available output signal amplitude, (c) trigger sensitivity (minimum trigger voltage), (d) power dissipation, and (e) stability. Based on this discussion, we will show that an integrated TELD-FET unit is potentially a preferred geometry. We will compare various TELD geometries and present a self-consistent design procedure for a TELD-FET combination. Experimental results based on the use of discrete TELDs and FETs are very encouraging.

2.2 Critical Limiting Factors

A. RC TIME CONSTANTS

Figure A-1 shows a simple TELD pulse generator. The low-field resistance of the device is R_1 and the load resistor value is R_L. The device is subcritically biased (i.e., below $V_{th} = E_H \ell_{ca}$). A negative pulse applied at the gate increases the electric field under the gate to above threshold value and nucleates a domain. The device current drops, and an output voltage is generated across the load. This output voltage is then used to trigger the following logic gates. Figure A-2 shows an equivalent circuit of Fig. A-1. The shunt capacitance C_{sh} comprises the total input gate capacitances of the following logic gates and the associated interconnect line capacitances. When a dipole domain is triggered in the subcritically biased device by the application of an input gate pulse, a domain is generated that travels along the sample and is extinguished at the anode. After the domain disappears, however, the voltage at the cathode rises to the quiescent voltage level with a time constant determined by the charging

7. H. Yanai and T. Sugeta, "Some Features and Characteristics of Gunn Effect Digital Device," Jap. IECE Natl. Conv. Rec. No. 717, p. 808, Sept. 1969.

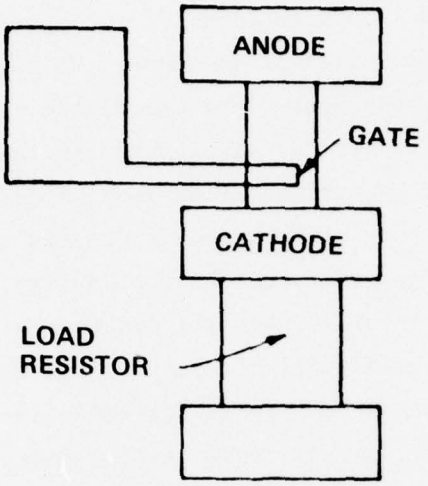

Figure A-1. Simple TELD pulse regenerator.

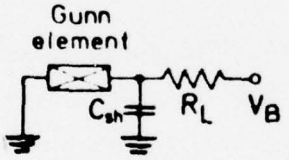

Figure A-2. Equivalent circuit of Fig. A-1.

time of the capacitance in parallel with the load resistor. This load resistor is equal to or larger than the device's low-field resistance, i.e.,

$$R_L \geq R_1 = \frac{\ell_{ca}}{ne\mu dW}$$

where ℓ_{ca} = cathode-anode distance
n = doping density
μ = low-field mobility
d = channel thickness
W = device width

The input gate capacitance C_g is given by

$$C_g = \sqrt{\frac{\varepsilon e n}{2V}}\ \ell_g W$$

where ε = dielectric constant

V = reverse bias on the gate

ℓ_g = gate length

For a fan-out of two, $C_{sh} = 2\ C_g$ (neglecting the interconnect capacitance). The charging time T is therefore given by

$$T = 2\ R_L C_g$$

$$\geq 2\ R_l C_g$$

$$T \geq 2\ \frac{\ell_{ca}}{ne\mu dW}\ \sqrt{\frac{\varepsilon e n}{2V}}\ l_g W$$

$$\geq \sqrt{\frac{2\varepsilon}{neV}}\ \times\ \frac{\ell_{ca}}{\mu}\ \times\ \frac{\ell_g}{d}$$

For practical devices, $\ell_{ca} \simeq$ 10-30 μm, $\ell_g \simeq$ 2.0 μm, $n \simeq 10^{16} cm^{-3}$, $\mu \simeq$ 4000-6000 cm^2/V-s, d $\simeq$ 2 m, and V $\simeq$ 1-2 V.

$\therefore$ $T \geq$ 10-20 ps

The domain formation time is of the order of 5-15 ps. The charging time is therefore of the same order as the domain formation time. As a consequence, the voltage across the TELD remains above the threshold level *for a time interval after the domain is extinguished.* Therefore, a new domain is nucleated under the gate, the process of domain extinction and formation repeats, and the device stays in a memorized state. In actual circuits, parasitic capacitances increase the value of C_{sh} and hence the charging-time constant. To avoid this memorized state, the device has to be biased at a lower anode voltage. This results in both lower trigger sensitivity and lower output voltage. The RC

time constant has to be kept very low in order to achieve a reasonable fan-out capability.

B. PERCENTAGE CURRENT DROP

A Schottky-barrier-gate TELD is shown schematically in Fig. A-3. The dc equivalent circuit and the spatial dependence of electric field in the channel are also shown. It can be demonstrated that the device current I_o is given by

$$I_o = \frac{V_o}{R_1}\left[1 + \frac{\ell_g}{L}\left\{\frac{d_d/d}{1 - d_d/d}\right\}\right]^{-1}$$

where R_1 is the device resistance in the absence of Schottky gate, and V_o is the applied voltage across the device [8]. The electric field under the gate region E_G is given by

$$E_G = \frac{V_o}{\sigma_1 A R_1}\left[1 - \frac{d_d}{d}\left(1 - \frac{\ell_g}{L}\right)\right]^{-1}$$

where σ_1 = channel conductivity

$A = Wd$ = device-cross-sectional area

d_d = depletion region under the gate

The depletion region under the gate d_d is given by

$$d_d = 2\varepsilon\left[(V_G + V_B)/en\right]^{1/2}$$

where ε = dielectric constant

V_G = voltage applied on the gate

V_B = built-in diffusion potential

n = doping density

8. K. Heime, "Planar Schottky-Gate Gunn Devices," Electron. Lett. 7, 610 (1971).

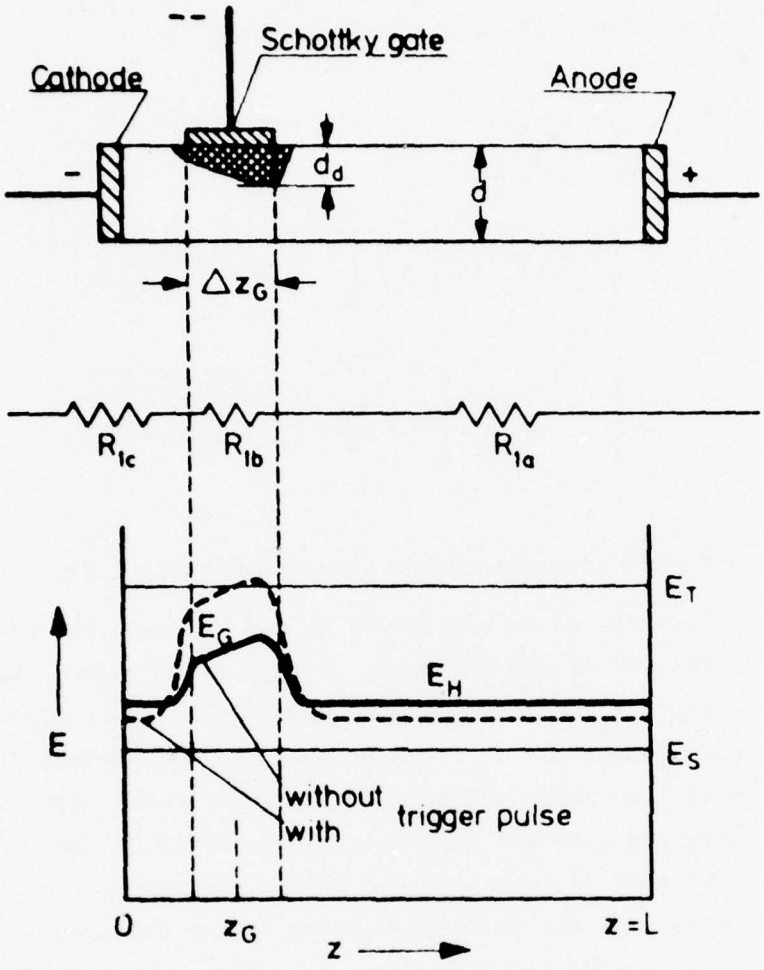

Figure A-3. Schematic representation of TE element with Schottky gate for domain triggering by field-effect action, and dc equivalent circuit. Spatial dependence of electric field E in "channel," without and with trigger pulse applied to gate.

In the quiescent state, the voltage V_o across the device is adjusted so that E_G is below threshold value. The quiescent current I_o is less than the threshold current; the actual value depends on the fractional *depletion region under the*

gate (d_d/d). The valley current $I_V = ne\, v_{sat} A$, where v_{sat} is the saturated electron velocity. The current dropback is given by

$$\frac{I_o - I_v}{I_o} = \left(1 - \frac{I_v}{I_o}\right)$$

$$= \left\{1 - \left(\frac{ne\, v_{sat}\, A}{\frac{V_o}{L}\, ne\mu_1\, A}\right)\left[1 + \frac{\ell_g}{L}\left(\frac{d_d/d}{1 - d_d/d}\right)\right]\right\}$$

$$\leq \left\{1 - \frac{v_{sat}}{v_{peak}}\left[1 + \frac{\ell_g}{L}\left(\frac{d_d/d}{1 - d_d/d}\right)\right]\right\}$$

When $\ell_g \to 0$, $\frac{I_o - I_v}{I_o}$ represents the fractional current drop in a two-terminal terminal TED. From the above expression it can be seen that the *fractional current drop increases if* (i) *the anode voltage is increased,* i.e., $V_o/L \to E_{th}$; (ii) *the gate length* ℓ_g *and/or depletion layer depth* d_d *is decreased;* and (iii) *the carrier concentration is decreased, and the channel thickness* d *is increased.* As will be shown below (see C) some of these requirements are contrary to those required for good trigger sensitivity. Therefore, a compromise has to be made in selecting the device parameters.

It is evident from the above discussion that a two-terminal TELD will provide a much larger fractional current drop than will an equivalent three-terminal Schottky-barrier-gate TELD.

C. TRIGGER SENSITIVITY (MINIMUM TRIGGER VOLTAGE)

A three-terminal TELD is schematically shown in Fig. A-4. A proper choice of the device geometry (i.e., dimensions) and material parameters has to be made for good device performance. We will now discuss how the trigger sensitivity is related to the material characteristics and device dimensions.

The device designs discussed by Sugeta et al. [4] and Mause et al. [1] have many limitations. First, the external charging-time constant is rather high, and therefore we cannot make use of the small (5-15 ps) domain formation times in these devices. Second, Sugeta et al. [4] assumed that the minimum increase

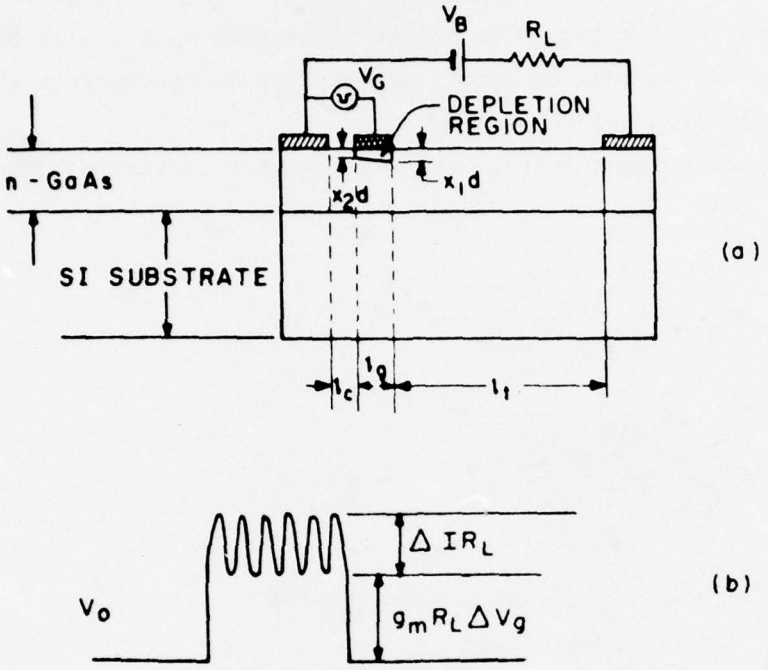

Figure A-4. (a) Schematic of device structure. (b) Output voltage V_o for a wide input pulse.

in electric field ΔE_m necessary for domain triggering in a TELD is equal to the electric field generated by the noise fluctuations in the carrier density. In the actual experimental work reported [1,5,9] the bias voltage was selected so that the maximum electric field in the device was about 0.9-0.95 times the threshold field. Schokley's gradual approximation theorem shows that the maximum field in a Schottky-barrier-gate TELD exists under the anode edge of the Schottky gate. Therefore, in the subthreshold case (when the device is not exhibiting transit-time oscillations) the maximum electric field under the gate is about 0.9-0.95 E_{th}. The negative-input-signal voltage applied to the gate must be large enough to raise the electric field in this region to a value above the threshold for domains to form. Thus, the increase in the electric field, E, required is about 0.05-0.1 E_{th}. A load resistor R_L is generally used

9. J. Allen, "Computer Architecture for Signal Processing," Proc. IEEE 63(4), 624-732 (1975).

in series with the device to develop an output signal, and a constant voltage supply is used for biasing. The trigger sensitivity of the TELD, including the influence of the load resistor, was studied by Upadhyayula [10]. The results are summarized briefly below.

The minimum trigger voltage ΔV_g required for nucleating domains in a TELD is given by [10]

$$\Delta V_g \leq \frac{0.2x_{1th}\,(1 - x_{1th})\phi_p}{(1 + g_m R_L)} \tag{1}$$

or

$$\Delta V_g = \frac{0.2\phi}{(1 + g_m R_L)} \left(\frac{1}{x_{1th}} - 1\right) \tag{2}$$

where ϕ = reverse bias on the Schottky gate

ϕ_p = pinch-off voltage

and x_{1th} = depletion-layer thickness at the anode edge of the Schottky gate normalized to the active-layer thickness d. The built-in diffusion potential for GaAs Schottky barriers ϕ_b is about 0.8 V. Standard photolithographic techniques used in the device fabrication will limit cathode-to-gate spacing ℓ_{cg} to 1-2 μm and gate length ℓ_g to 2.0 μm. Therefore, for most of the practical devices, $\phi \simeq 2.0$ V. The trigger sensitivity curve for ϕ = 2.0 V from Ref. 10 is reproduced in Fig. A-5, where $g_m R_L$ represents the voltage gain of the device for below-threshold operation. The trigger sensitivity increases by a factor $(1 + g_m R_L)$ when the device has a good low field, g_m.

When biased below threshold field, a TELD operates in a manner similar to that of a Schottky gate or junction FET. From Bockemuehl's analysis on JFETs, g_m is given by [11]

$$g_m = \frac{W}{\ell_g} ne\mu d \quad [x_{1th} - x_{2th}] \tag{3}$$

where $ne\mu = \sigma$, and the other parameters were defined earlier. If standard

10. L. C. Upadhyayula, "Trigger Sensitivity of Transferred Electron Logic Devices (TELDs)," IEEE Trans. Electron Devices ED-23, 1049-1052 (Sept. 1976).
11. R. R. Bockemuehl, "Analysis of Field-Effect Transistors with Arbitrary Charge Distribution," IEEE Trans. Electron Devices ED-10, 31 (1963).

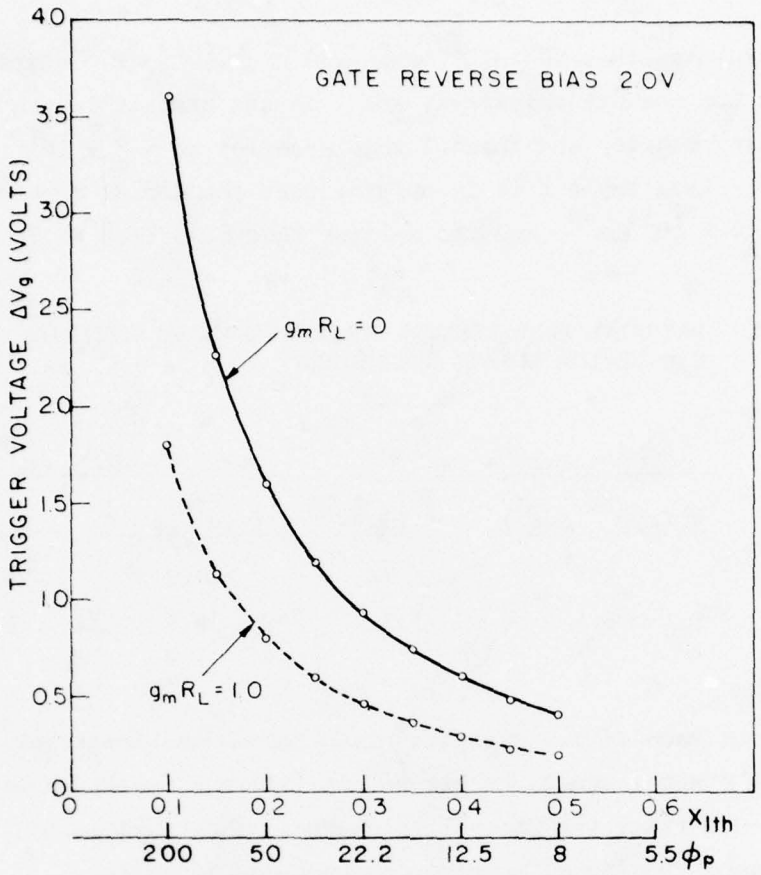

Figure A-5. Trigger sensitivity of a TELD as a function of fractional depletion width (x_{1th}) or pinch-off voltage (ϕ_p) for d = 2.0 V. The nd is kept constant and both n and d are allowed to vary; $g_m R_L$ is used as a parameter.

photolithographic techniques are used in the device fabrication, $\ell_{cg} \simeq$ 1-2 μm and $\ell_g \simeq$ 2.0 μm. For Schottky barriers on GaAs, the built-in potential $\phi_b \simeq$ 0.8-1.0 V. If the material parameters are selected so that nd $\simeq 2 \times 10^{12}$ cm^{-2} with n $\simeq 2 \times 10^{16}$ cm^{-3} and $\mu \simeq$ 5000-5500 $cm^2/V\text{-}s$, g_m can be computed from Eq. (3) for any W/ℓ_g ratio. The transconductance g_m can be shown to be 5 mmho for $W/\ell_g = 50$, and 10 mmho for $W/\ell_g \simeq 100$. The device low-field resistance turns out to be in the 30-70-Ω range; this allows load resistance (R_L) values of about 100 Ω. For an R_L of 50-100 Ω and g_m of 5-10 mmho we obtain $g_m R_L$ values of 0.25-1. This explains our choice of $g_m R_L$ values of 0 and 1 in Fig. A-5. The trigger sensitivity for practical devices therefore lies between the two curves of Fig. A-5. A desirable value for trigger sensitivity ΔV_g is between 0.5 and 1.5 V. This corresponds to a pinch-off voltage ϕ_p of 22-50 V. It has been established

from domain dynamics that $nd \geq 10^{12}$ cm^{-2} and $n\ell \geq 10^{13}$ cm^{-2} where n is the doping density, d is the channel thickness, and ℓ is the transit length [1]. Table 1 shows the doping density and channel thickness for $nd \simeq 2 \times 10^{12}$ cm^{-2} and 4×10^{12} cm^{-2}. From Table 1 it is evident that the doping density should range from 0.6 to 5.2 x 10^{16}cm^{-3}, and the n-layer thickness from 0.77 to 3.5 μm.

TABLE A-1. MATERIAL REQUIREMENTS FOR CONVENTIONAL TELDs AS PER OUR NEW DEVICE DESIGN GUIDELINES

ϕ_p	nd = 2x10^{12} cm^{-2}		nd = 4x10^{12} cm^{-2}	
(V)	n (x10^{16} cm^{-3})	d (μm)	n (x10^{16} cm^{-3})	d (μm)
22.0	1.3	1.54	5.2	0.77
50.0	0.6	3.5	2.9	1.75

The trigger sensitivity analysis presented above shows that (i) the doping density in the channel should be higher and (ii) the depletion under the gate should be 0.2-0.3 times the channel thickness. *These requirements are contrary to those for good fractional current dropback and stability.*

D. FAN-OUT

In simple sequential circuits (e.g., dynamic shift registers or ring counters) a number of devices are connected in series so that the output of a device is used to trigger the succeeding one. Thus, only a fan-out of 1 is required. For a majority of digital-logic operations, however, a device has to trigger two or more devices, and a fan-out of 2 or more is required. It is, in general, desirable to have as large a fan-out capability as feasible in a logic family. We shall now consider the fan-out capability of TELDs and the constraints set up by fan-out considerations.

Fig. A-6 schematically shows a TELD driving m similar devices simultaneously, i.e., with a fan-out of m. In order to successfully trigger m similar devices, the TELD (acting as a pulse current generator) must provide an output pulse of sufficient amplitude to raise the E-field under the gates of the following m

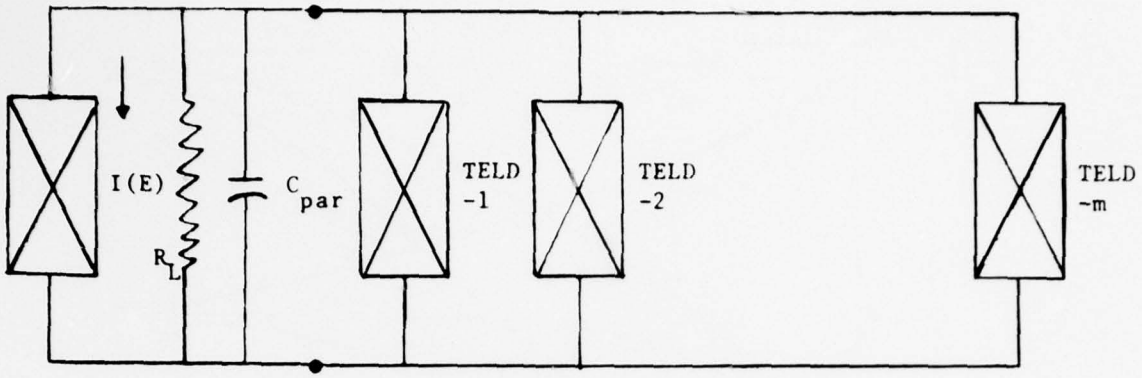

Figure A-6. TELD driving m-similar devices.

identical devices. The maximum value of m under the worst case conditions is called fan-out. The value of m depends on the ratio of load resistance R_L to low-field resistance R_l and the current gain factor ζ_{max}. The value of m is given by [7]

$$m = \frac{R_l(1 - \zeta_G) + R_{La}}{R_l + R_{La} + R_{Lc}} \left(\zeta_{max} - \frac{R_{Lc} + \zeta_G R_l}{R_{La}}\right) \tag{4}$$

where R_{La} = load resistor in the anode circuit

R_{Lc} = load resistor in the cathode circuit

$\zeta_G = \ell_{cg}/\ell$

A plot m as a function of R_{La}/R_l and R_{Lc}/R_l computed by Yanai and Sugeta [7] is shown in Fig. A-7. From this figure, it is clear that the fan-out is maximum when (i) the anode load resistor is equal to or larger than the device low-field resistance, (ii) the cathode load resistor is zero, and (iii) the trigger electrode is located close to the cathode. Reasonable values of R_L/R_l lie between 2 and 10.

E. CURRENT GAIN FACTOR

In order to discuss the current gain factor α_{max} one has to consider the dynamics of a mature high-field domain in a TELD. We will use the notation

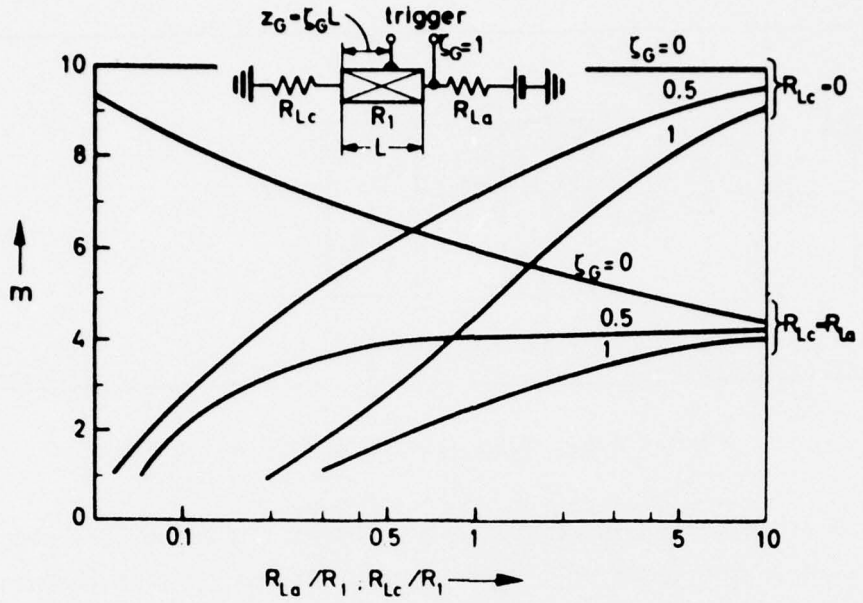

Figure A-7. Dependence of fan-out m on ratio of load resistance R_L to low-field sample resistance R_1 with distance between cathode and trigger gate as parameter, according to Eq. (4), with $\alpha_{max} = 10$. After Yanai and Sugeta [7].

and the excellent description presented in the book by Bosch and Engelman [12]. We shall consider "triangular" mature domains. In order to provide a readable description, Fig. A-8 shows the steady-state domain electric field and associated-carrier distribution. Several critical domain parameters are defined in the figure. Note that the subscript ∞ refers to steady-state values, $E_{1\infty}$ is the electric field outside the domain, $v_{1\infty}$ is the velocity corresponding to $E_{1\infty}$ and is equal to the domain velocity, and $E_{2\infty}$ is the domain peak field. The symbol E_h will be used to denote average value of the electric field; this is the device voltage divided by the device length (i.e., device terminal field).

The transferred-electron device is basically a current source. For logic applications, the device is biased below the threshold value of I_t. By applying a higher field, the current is increased by ΔI_{ta}. This causes domain nucleation and a decrease in the device output current of ΔI_t. The current

12. B. G. Bosch and R. W. H. Engelmann, *Gunn Effect Electronics*, John Wiley & Sons, Inc., New York, 1950.

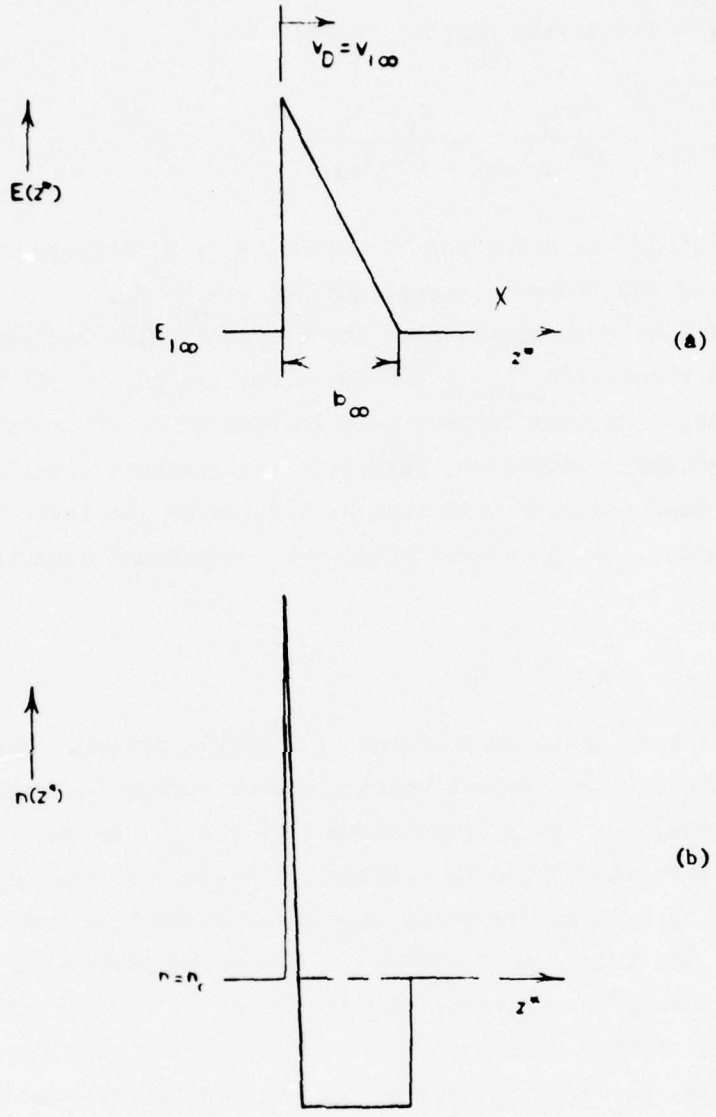

Figure A-8. (a) Electric field and (b) carrier profile of a mature triangular dipole domain.

gain factor α_{max} is given by the ratio of the amplitude of the output current pulse to minimum triggering current pulse; i.e.,

$$\alpha_{max} = \frac{\Delta I_t}{(\Delta I_{tA})_{min}} = \frac{E_T - E_{1\infty}}{(\Delta E_A)_{min}}$$

E_T is the threshold field for the TE effect, $E_A = V_A/L$ where V_A is the applied voltage and L is the transit length, and $\Delta E_A = E_A - E_T$.

For $n\ell$ product much higher than the critical value and small R_L, $E_T - E_{1\infty} \simeq 2.8$ kV/cm, $(\Delta E_A)_{min} \simeq$ 100-300 V/cm, and $\Delta I_t \simeq 0.55\ I_o$ where I_o is the peak current. Maximum current gain factors of 10-20 are therefore possible.

Under realistic conditions, parasitic capacitances shunting R_1 are always present. The load resistor will also be shunted by the input capacitance of the succeeding stages. For a fan-out of m, the total shunt capacitance C_{sh} is given by

$$C_{sh} = C_{par} + m\ C_g$$

where C_g is the input gate capacitance of a single device. Due to this shunt capacitance, the device terminal voltage cannot change instantaneously after domain extinction, but has a time constant of $R_L C_{sh}$. As described earlier, this tends to keep the device in a memorized state. To ensure only single-domain triggering by a narrow input pulse, the anode bias and hence I_o have to be decreased. The triggering current ΔI_A has to be increased, resulting in smaller α_{max}. *Thus, the presence of parasitics and loading capacitances results in having to operate in a region of low current gain for stable operation.* Similarly, to obtain increased fan-out capability, one has to trade off current gain capability.

Figure A-9 shows α_{max} as a function of R_L with C_{sh} as parameter [13]. For shunt capacitances in the range of 0.05-0.1 pF, R_L values of 200-300 Ω are the maximum permitted. This represents a reasonable range for R_L for realistic values for material parameters and forms a starting point for design. As

13. T. Sugeta et al., "Gunn Effect Functional Device, Repr. No. 45-11, Meeting Jap. IEE Prof. Group on Transistors, Sept. 1970.

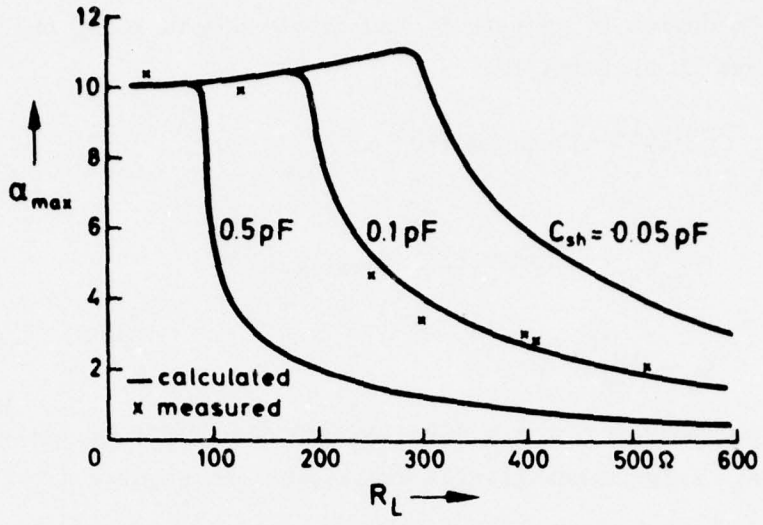

Figure A-9. Dependence of maximum current gain α_{max} on ohmic load resistance R_L with parasitic capacitance C_{sh} as parameter. R_1 = 100 Ω, $n_o = 10^{15}$ cm^{-3}, L = 100 μm, static sample capacitance C_h = 0.015 pF. After Sugeta et al. [13].

discussed in D, fan-out considerations suggest a ratio of device to load resistance of 0.1-0.5. Thus, the device low-field resistance should be about 30-100 Ω.

F. DEVICE DISSIPATION

The short rise and fall time and small propagation delay associated with TELDs can be utilized for high-speed logic applications only if monolithic integration is achieved. Small parasitic capacitances and low-resistance circuits are required to keep the RC time constants small. On the other hand, a reasonably high packing density implies low power dissipation per device.

In the quiescent state, a TELD is biased near threshold value, and the power dissipation is given by

$$P_{th} = e\mu n E_{th}^2 LWd$$

and the low-field resistance R_1 is given by

$$R_1 = L(e\mu n \ell c)W$$

where all the parameters have been defined earlier.

For the device to operate in the dipole-domain mode, the following criteria have to be fulfilled:

$$nL > 10^{13}\,cm^{-2} \text{ and } nd > 10^{12}\,cm^{-2}$$

Therefore,

$$(P_{th})_{min} = \frac{1.5 \times 10^{17}}{n} \text{ W watts/cm}$$

and

$$R_1 = \frac{10^{16}}{nW} \ \Omega$$

Here electron mobility of $\mu = 6000\ cm^2/V\text{-}s$ and threshold field $E_{th} = 4$ kV/cm are assumed. Trigger sensitivity considerations require $n \simeq 2 \times 10^{16}\,cm^{-3}$. Hence,

$$P_{th,min} = 0.75 \text{ W milliwatt}$$

and

$$R_{1,min} = \frac{5000}{W} \ \Omega$$

where W is the device width in microns. A cathode-to-anode spacing of 10 μm is used in the above calculation. During the discussion on fan-out and current gain of a TELD, it has been shown that R_1 of the order of 30-100 Ω is desirable. This leads to a channel width of 50-150 μm and device dissipation of 40-100 mW. Of course, the dc dissipation in the load resistor is at least of the same magnitude. *The power dissipation in a TELD-linear load resistance unit will thus be of the order of 80-200 mW, values which are in good agreement with the published experimental results.*

G. MINIMUM DEVICE DIMENSION FOR TELD MSI CIRCUITS

We now consider minimum device dimensions for TELD MSI circuits. The discussion will be for three-terminal Schottky-barrier-gate TELDs with linear load resistors. It will be shown that earlier estimates for device size and consequently power dissipation and packing density were overly optimistic. These optimistic estimates are a result of using *single-device* considerations and ignoring constraints set up by the need to obtain stable operation (without self-triggering) and to drive other logic gates with reasonable fan-out. It

should be noted that even the internal logic gates in an MSI implementation must be capable of charging the input capacitance of a succeeding gate (or preferably gates for fan-out greater than unity) without serious degradation in pulse rise time. As we have shown earlier, rise-time degradation can cause self-triggering and hence unstable operation. Furthermore, rise-time degradation defeats our purpose and slows down the rate at which logic can be performed.

The criteria for TELDs to find use in multigigabit-rate MSI circuits are the following:

1. Multigigabit-rate operation capability.
2. Minimum power dissipation to achieve high packing density.
3. Stable operation - i.e., no self-triggering unless expressly desired.
4. Capability to charge interconnect lines, input capacitance of succeeding gates, and parasitic fringing capacitances without serious degradation of rise time.
5. High trigger sensitivity.

These conflicting requirements impose restrictions on the minimum device size.

From a general understanding of the TELDs, one can conclude that GaAs wafers with 1-2 x $10^{16}cm^{-3}$ doping density are most suitable. For the purpose of discussion, let us assume that $n = 10^{16}cm^{-3}$, $\mu \underline{\sim} 6000\ cm^2/V\text{-}s$, $d = 1.0\ \mu m$, and $E_{th} = 4$ kV/cm. Hence, the device dissipation P_{th} and low-field resistance R_l are given by

$$P_{th} = 1.5\ W \text{ milliwatt}$$

$$R_l = \frac{10^4}{W}\ \Omega$$

while $nd = 10^{12}\ cm^{-2}$

$n\ell = 10^{13}\ cm^{-2}$

are assumed.

From purely power dissipation considerations one would like to choose as small a value for W as possible. A small value for W, however, implies a large device resistance R_1 and hence a large load resistor that will increase the external circuit time constant.

For the sake of argument let us assume that W = 10 μm [1].

$$\therefore \quad P_{th} = 15 \text{ mW and } R_1 = 1.0 \text{ k}\Omega$$

As discussed earlier, the subthreshold transconductance g_m for such small devices is nearly zero. The pinch-off voltage for the channel under consideration is about 8.0 V. For a gate reverse bias of 2 V, the minimum signal required for gate triggering, as per Ref. 10, is

$$\Delta V_g = 0.5 \text{ V}$$

For the successful operation of TELDs, the gate trigger sensitivity should be better than the anode trigger sensitivity ΔV_A.

$$\frac{\Delta V_A}{\Delta V_g} \geq 1.0$$

For a 10-μm-long device, $V_{th} \simeq 4.0$ V; when the anode bias is 0.9 V_{th} in the quiescent state, $\Delta V_A \simeq 0.1\ V_{th} \simeq 0.4$. For most experimental devices it has been found that $\Delta V_A \simeq 0.15\ V_{th}$ is required instead of $0.1\ V_{th}$. Even if we use the optimistic value for ΔV_A we have

$$\frac{\Delta V_A}{\Delta V_g} \simeq \frac{0.4}{0.5} = 0.8$$

This ratio is less than unity and seriously affects the stability. The voltage across the TELD exceeds the threshold value when a domain is formed. *This voltage pulse should decay with a time constant smaller than the domain formation time, otherwise domain nucleation and absorption process repeats continuously even when the input trigger pulse is removed.* When $\Delta V_A >> \Delta V_g$, the output amplitude required for the following gates is small and, therefore, when this pulse rides on the dc bias it cannot cause anode triggering.

This stability consideration is believed to be the reason why devices with 70-100-μm transit length are used in all the experimental research reported from Japan. The power dissipation achieved experimentally by these researchers is thus excessively high for MSI circuits. Mause et al. [1]

suggest the use of TELDs with 10-μm transit length and 10-μm width to obtain minimum power dissipation of 25 mW for a TELD-load resistor combination. All the experimental results on three-terminal TELDs quoted by Mause, however, were obtained with TELDs of 30-50 μm transit length. At RCA, we have decreased the transit length to 12-15 μm, but increased the device width W to increase subthreshold transconductance and improve gate-triggering sensitivity. Increasing W, however, prevents us from reducing the power dissipation to 25 mW.

(1) Load Resistance. In our discussion on fan-out D, it has been shown that the load resistor should be one to two times the device's low-field resistance to provide a fan-out of 2-3. Therefore, for the device under consideration, $R_L \simeq 2\ R_1 = 2\ k\Omega$.

(2) Gate Input Capacitance. The gate input capacitance C_g is given by

$$C_g = \sqrt{\frac{\varepsilon en}{2V}}\ \ell_g W$$

where ℓ_g is the gate length. For W = 10 μm, ℓ_g = 1.0 μm. V = 2.0, and $n = 10^{16} cm^{-3}$ we have C_g = 0.002 pF.

(3) Fringing Capacitance. Mause [1] pointed out that (i) the fringe capacitance to ground of TELDs and load resistor C_{fr} and (ii) interconnect transmission lines C_S of the same dimensions under consideration are not negligible. He estimated C_{fr} = 0.005 pF. *Even when the devices are integrated on the same chip, the interconnect line capacitances are not zero.* Due to the physical and thermal limitations, the separation between any two devices is about 100-150 μm. For a fan-out of 2, the interconnect line capacitance C_S = 0.003 pF. Therefore, for a fan-out of 2, the total capacitance to be charged or discharged is given by

$$C_{sh} = (C_{fr} + 2\ C_g + 2\ C_S)$$

$$= (0.006 + 2x0.002 + 2x0.003)\ pF$$

$$C_{sh} = 0.016\ pF$$

The charging time constant t_c is therefore given by

$$t_c = R_L C_{sh}$$

$$t_c = 2x10^{3} \times 0.016x10^{-12}$$

$$t_c \simeq 32\ ps$$

The time constant t_c is much larger than the domain formation times (5-15 ps), and hence the output generated across the device will not decay fast enough to suppress the successive domain formation.

The minimum device dimensions discussed by Mause [1] will, therefore, result in self-triggering and unstable operation. It should also be noted that the lower limits for $nd = nd_{crit}$ and $n\ell = n\ell_{crit}$ were used in the above calculations. From our own experience and other published data [14] we know that one has to use $nd \simeq 2\ nd_{crit}$ for obtaining an adequate percentage current drop (20-25%) in TELDs. This will increase the gate capacitance by a factor of $\sqrt{2}$ and dc dissipation by a factor of 2 and will reduce the load resistor by 2. As a consequence, the time constant t_c remains nearly the same, but the device dissipation will be 30 mW instead of 15 mW. Also, the current gain calculations of Sugeta et al. [13] indicate that load resistance values greater than 300 Ω are not suitable for TELD circuits.

We, therefore, conclude that a minimum device width of about 50 μm is required for TELDs used in MSI circuits. This applies to conventional three-terminal TELDs with linear load resistors. This will result in a TELD-load resistor unit dissipating about 100 mW. Means of decreasing load resistor requirements and improving trigger sensitivity by the use of capacitive pickoff output and FET-type triggering sections will be discussed below.

2.3 TELDs With Capacitive-Output Electrode

The TELD circuits described earlier used linear load resistors. The linear load resistors may be replaced by active devices (e.g., MESFETs or dielectrically loaded TELDs) working as nonlinear load resistors. This can reduce the external RC time constants, but does not completely eliminate them. Also, the output is taken across the TELD. Therefore, when a fan-out of 2 or more is required, the device may go into the memorized (oscillatory) state instead of remaining in the desired (triggered) single-domain mode. Furthermore, the preferred mode of operation of TELDs in logic circuits is the common cathode configuration (i.e., load resistor on the anode side). Even

14. K. Mause et al., "Circuit Integration with Gate Controlled Gunn Devices," Proc. 4th Int. Symp. GaAs and Related Compounds, Boulder, Colo., Sept. 1972, pp. 275-285.

though the output signal amplitude is similar to the input required to trigger the next TELD, the actual voltage levels are different. Compatibility of input and output pulses can be restored by incorporating a dc shifter or through ac (capacitive) coupling. The dc-level-shifter network consumes considerable power and is not very suitable for MSI or LSI circuits. As the transit-time frequency of TELD is in the 3-10-GHz range, capacitive coupling is feasible without the use of bulky coupling capacitors. Instead of developing the output across a load resistor and then capacitively couple it to the succeeding stages, one can use a capacitive-pickoff-output electrode on the TELD itself. In fact, this technique was used to measure the domain potentials in TEDs. Mause [15] used planar TELDs with capacitive-pickoff electrode for demonstrating multiplexing and demultiplexing techniques at 1.8 gigabit rates. Figure A-10 shows a TELD with a capacitive pickoff output. The anode, cathode, and Schottky-gate construction is similar to that of standard TELDs. The pickoff electrode is a narrow metal stripe isolated from the device active region by a thin dielectric layer of SiO_2 or SiO or Al_2O_3. The TELD is biased below threshold, and domains are nucleated by the application of a negative signal to the Schottky-barrier input gate. When the domain is in transit between the gate and the output electrode, the potential under the capacitive-pickoff electrode increases and a positive pulse appears at the output. When the domain is in transit between the output electrode and anode, the potential under the output electrode drops and a negative pulse appears at the output. The capacitive-pickoff probe essentially samples the domain voltage as the domain passes under it. Either the positive or negative output pulse can be used for triggering succeeding stages. The device delay is equal to the domain formation time when the positive pulse is used. A throughput delay equal to the domain transit time from input gate to output electrode occurs when the negative pulses are used for triggering the succeeding stages. *But the maximum frequency at which these circuits work is still given by the transit-time frequency that corresponds to the cathode-anode spacing.* Since the output is taken neither from the cathode nor anode, memory action will not take place in this device and true, stable single-domain operation will be possible.

15. K. Mause, "Multiplexing and Demultiplexing Techniques with Gunn Devices in the Gigabit-Per-Second Range," IEEE. Trans. Microwave Theory Tech. MTT-24(12), 926 (Dec. 1976).

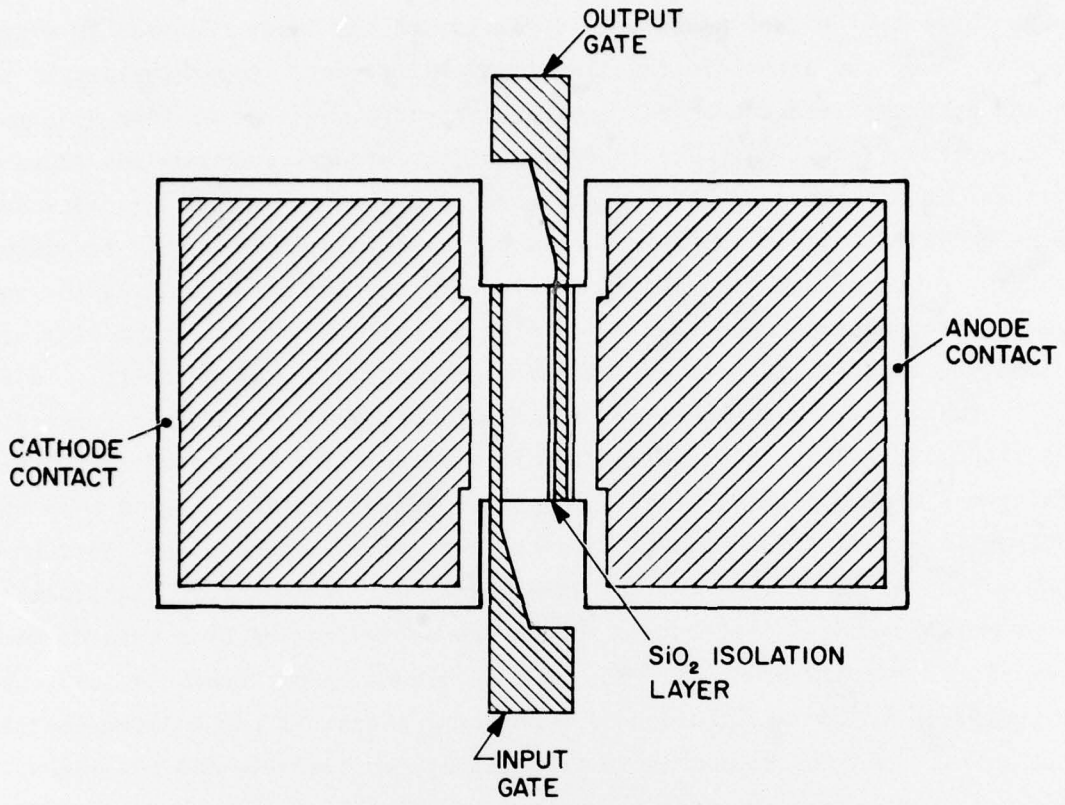

Figure A-10. Schematic of TELD with capacitive pickoff output.

The output voltage amplitude for a capacitive pickoff is given by

$$\Delta V_o = \alpha K V_{th}$$

where

α = coupling coefficient

K = percentage current drop

V_{th} = threshold voltage

Mause [15] pointed out that α is of the order of 0.75 when a TELD is driving a split-gate TELD. Even though K = 0.5 is theoretically possible, the best experimental values lie in the 0.3-0.35 range. An output voltage of 1.0 is generated when the threshold voltage is about 5.0 V (i.e., $\ell_{ca} \simeq 15$ μm). The value of the coupling coefficient decreases when the capacitive loading is increased (i.e., for fan-out greater than 1) and the output amplitude decreases. This can be made up to some extent (at the cost of dc dissipation) by increasing the cathode-anode length.

For high-speed logic applications, the anode bias on a TELD (i.e., between cathode and anode) is just below threshold value. For well-defined domain formation, the voltage across the device has to be increased to a level well above the threshold. This can be realized by including a resistor in series with the device. When the domain forms, the device current decreases. The voltage drop across the resistor decreases, causing the voltage across the device to increase to well above threshold level. Thus, even with capacitive-output electrodes a load resistor is desirable. This, of course, will consume dc power.

2.4 Integrated TELD-FET Structure with Capacitive-Output Electrode

The power-optimized TELD with the capacitive-pickoff electrode described in Section 2.3 still suffers from (i) relatively poor trigger sensitivity and (ii) current drop smaller than that in a comparable two-terminal TED. The major advantage of this structure is the elimination of self-triggering when single-domain operation is desired. Furthermore, the use of the capacitive pickoff allows input/output compatibility, and hence makes possible the direct cascading of logic gates without level shifting in both common anode and common cathode configurations. Some of the problems can be minimized by the use of an integrated TELD-FET structure. Preliminary experimental results obtained with a combination of discrete FETs and TELDs are very encouraging.

The basic principle of this structure is to use current matched FET and two-terminal TELD structures in series. For a given current level, an FET can be made with a larger W/ℓ_g, resulting in a higher transconductance and hence better trigger sensitivity. As discussed in Section 2.2, a two-terminal TELD has a higher current drop than a comparable three-terminal device and thus provides a larger output voltage. Furthermore, the voltage across the FET is lower than that in a linear load resistor. Figure A-11 shows a schematic of an integrated TELD-FET with a capacitive-pickoff electrode. A first-order design procedure is now presented.

GaAs FETs are used for microwave amplifiers and oscillators. For power FET, GaAs wafers with 8-10 x 10^{16} cm^{-3} doping density are generally employed.

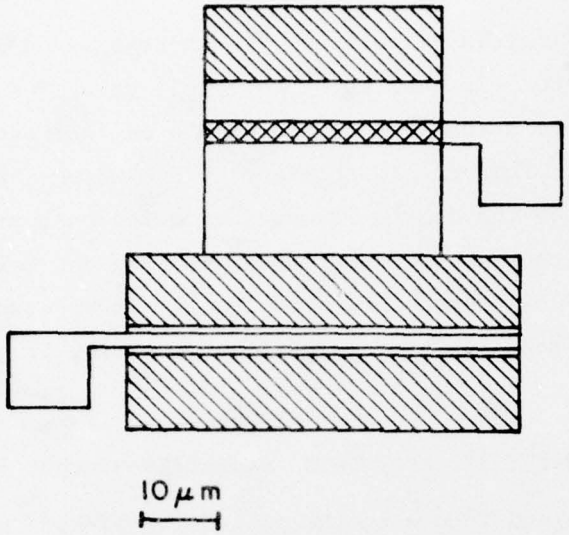

Figure A-11. Schematic of an integrated TELD-FET with a capacitive-pickoff electrode.

However, Hower et al. [16], Futkuta et al. [17] and Napoli et al. [18] used wafers with doping densities in the 2-4 x 10^{16} cm^{-3} range and reported good FET performance. Transferred-electron logic devices require electron mobilities in the 5000-5500-cm^2/V-s range so that the electrons can reach close to the peak velocities of 2 x 10^7 cm/s at the threshold field. Therefore, we will use GaAs with 2 x 10^{16} cm^{-3} doping density, 1-μm channel thickness, and 5500-cm^2/V-s mobility. We will compute the device geometries required for both FET and TELD from first-order theories so that they can be fabricated in an integrated form.

16. P. L. Hower and N. G. Bechtel, "Current Saturation and Small-Signal Characteristics of GaAs Field-Effect Transistors," IEEE Trans. Electron Devices ED-20, 213-220 (Mar. 1973).
17. M. Fukuta, T. Mimura, I. Tujimura, and A. Furumoto, "Mesh Source Type Microwave Power FET," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 1973, pp. 84-85.
18. L. S. Napoli et al., "High Power GaAs FET Amplifier - A Multigate Structure," in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 1973, pp. 82-83.

A. FET SECTION DESIGN

There are many procedures available for designing FETs. Fair [19] developed a graphical procedure for the estimation of the FET parameters. These procedures and associated mathematical relationships (for extrapolations) are used in our computation.

We will assume the following parameters:

Doping density, n	=	2×10^{16} cm^{-3}
Channel thickness, d	=	1.0 μm
Gate length, ℓg	=	1.0 μm
FET channel width	=	50 μm
Electron mobility at 300K	=	5500 $cm^2/V\text{-}s$

The pinch-off voltage U_o can be calculated to be 14.5 V. Following Fair's notation, the normalized gate voltage η is given by

$$\eta = \frac{V_G + V_B}{U_o} = 0.186$$

and

$$\eta_s = \frac{V_B}{U_o} = 0.048$$

A built-in diffusion potential $V_B = 0.7$ V is assumed. The drain-saturation current (I_{DSS}) curves of Fig. 4 of Fair [19] are given for pinch-off voltages up to 10 V. Therefore, Eq. 10 (which Fair used to generate these curves) was used to compute I_{DSS} as given by

$$I_{DSS} = \frac{G_o U_o [1 - \exp(-\Gamma')]}{(\Gamma')^2} \cdot \frac{h_D}{d}$$

where $\frac{h_D}{d}$ = normalized channel thickness at the drain end of the gate

$G_o = dne\mu W/\ell_g$ = channel conductance

$$\Gamma' = U_m \Gamma = U_m \frac{V_o}{\ell_g E_C}$$

and

$$U_m = \left(\frac{V_{sat} + V_B}{U_o}\right)^{1/2}$$

19. R. B. Fair, "Graphical Design and Iterative Analysis of the DC Parameters of GaAs FETs," IEEE Trans. Electron Devices ED-21(6), 357 (June 1974).

From Turner and Wilson's theory [20], $V_{sat} \simeq 0.14 U_o \simeq 2.0$ V. This number agrees fairly well with the experimental result of Napoli et al. [18]. Hence, we obtain

$$U_m = 0.43, \quad G_o = 0.08 \text{ mho}, \quad \text{and } \frac{h_D}{d} = 0.57$$

From the above expression, I_{DSS} is computed to be 19.3 mA. The gate will, however, be reverse biased by 2.0 V so as to decrease the gate capacitance and not to forward-bias the Schottky-barrier gate when the positive trigger signal is applied. Therefore, for 2.0 V reverse bias on the gate the FET quiescent current I_{DS} is given by

$$I_{DS} = I_{DSS}\left(\frac{1-\eta}{1-\eta_s}\right)$$

$$= 13.5 \text{ mA}$$

The transconductance $g_{m,sat} \simeq 4.2$ mmho for 2-V reverse bias on the gate

$$g_m = g_{m,sat} \frac{\eta_s^{1/2}}{\eta^{1/2}} = 2.0 \text{ mmho}$$

The gate capacitance of the FET, $C_g = 0.012$ pF.

B. TELD SECTION DESIGN

The TELD has to be designed so that its threshold current is higher than the FET drain-saturation current I_{DS}, and so that its valley current is considerably smaller than the drain-saturation current I_{DS}. The TELD cathode-anode spacing has to be chosen so as to provide a domain voltage of substantial value. The dimensions of the capacitive pickoff electrode are chosen so that a large portion of the domain voltage can be coupled to the following input gates.

20. J. A. Turner and B. L. H. Wilson, "Implications of Carrier Velocity Saturation in a Gallium Arsenide Field-Effect Transistor," in Proc. 2nd Int. Symp. Gallium Arsenide, Dallas, Tex., Oct. 1968.

(i) TELD Width. TELD is fabricated on the same epi-channel as FET. The TELD's material parameters are fixed; its width, therefore, is chosen as an adjustable parameter to match TELD and FET currents.

Since $I_{th} > I_{DS}$ and $I_v < I_{DS}$ and $I_{DS} = 13.5$ mA, we have chosen I_{th} to be 14 mA.

$$I_{th} = 14 \times 10^{-3} = nev_{th}dW'$$

where W' = TELD channel width

v_{th} = peak velocity and is equal to 2×10^7 cm/s for GaAs. The values for n and d are the same as in FET.

$$W' = \frac{I_{th}}{nev_{th}d} \approx 22\ \mu m$$

(ii) TELD Channel Length. The output voltage at the capacitive pickoff is given by

$$\Delta V_o = \alpha K V_{th}$$

where α = coupling coefficient

K = percentage current drop

$V_{th} = \ell E_{th}$ = threshold voltage

and E_{th} = threshold field for TE effect

As will be shown in (iii), α is of the order of 0.25-0.4. For exceptionally good epitaxial layers, K is of the order of 0.4 for cw operation. Mause [15] and Yanagisawa et al. [6] experimentally obtained 0.3-0.35 for K. For a channel length of 20 μm, $V_{th} \approx 7.2\text{-}8.0$ $\Delta V_o = 0.54\text{-}0.95$ V.

(iii) Coupling Coefficient (α). When a capacitive pickoff output is used, the voltage across the domain capacitance C_d is fed to the FET gate C_g through the coupling capacitance of the capacitive electrode C_c. A simple equivalent circuit is shown in Fig. A-12. For effective coupling, we should satisfy the following relations:

$$C_c > C_d$$

$$C_g < C_d$$

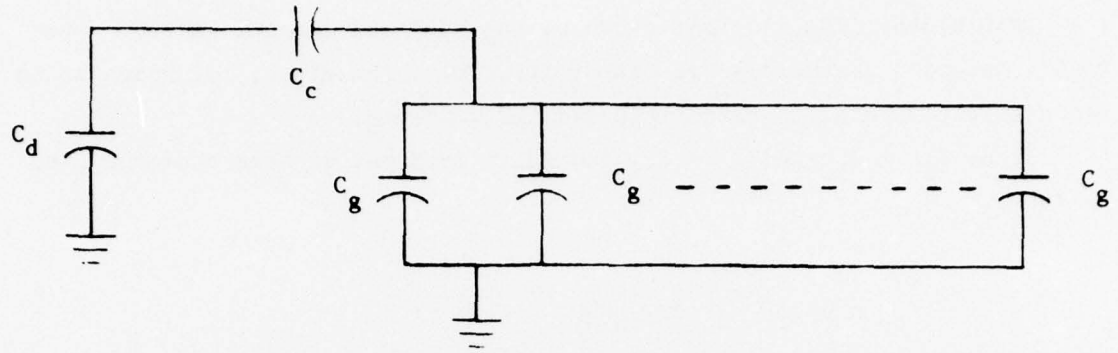

Figure A-12. Equivalent circuit of structure shown in Fig. A-11, when the output is driving several similar devices.

C_g was found to be about 0.012 pF. The domain capacitance is given by

$$C_d = \frac{2\varepsilon}{b} W'd$$

where 2 is used to account for the dielectric effects of the substrate. The domain width b is given by

$$b = \sqrt{\frac{2\varepsilon}{en|\mu'|}\left(\mu E_{th}\frac{\ell}{3}\right)}$$

where μ' = differential mobility $\sim$ 2000 $cm^2/V\text{-}s$.

Substituting the proper values for all the parameters, C_d is found to be 0.008 pF.

Assuming the length of the capacitive probe to be 3 μm, the width 22 μm, and dielectric film thickness 0.15 μm, we have

$$C_c = \frac{\varepsilon}{d} A$$

For silicon monoxide, C_c = 0.034 pF; for alumina ($A\ell_2O_3$), C_c = 0.059; and for SiO_2, C_c = 0.009 pF.

When silicon monoxide or alumina is used, one can obtain a sufficiently large coupling capacitance. When the coupling capacitance is large, the coupling coefficient α is given by

$$\alpha = \frac{C_d}{C_d + ZC_g}$$

Where Z = fan-out, α has a value of 0.4 and 0.25 for Z = 1 and 2, respectively. When split-gate devices are used along with clock inputs or coincidence inputs (AND circuits), the gate capacitance of the FET will be reduced by a factor of 2 (from 0.012 to 0.006 pF). The coupling coefficient improves considerably in this situation. Of course, the fringing capacitances and interconnect capacitance will somewhat reduce α again.

The transconductance of the input FET section of this integrated structure is 2 mmho, and the low-field resistance of the two-terminal TELD section is about 500 Ω. Consider an input signal of 0.75 V at FET gate. The output voltage change across the FET source-drain, $g_m \Delta V_g R_l$, will then equal 0.75 V. This corresponds to the increase in voltage across the TELD. As this increase is greater than 0.1 V_{th}, and as there is also an increase in current over the threshold level, domain nucleation takes place. Note that the TELD is only a two-terminal device, and thus the maximum current drop corresponding to material parameters can be achieved. A 3.5-V bias is required for the FET and a 6.5-V bias for the TELD, corresponding to a total bias voltage of 10 V. The power dissipated in this TELD-FET device is 135 mW. No additional load resistors are necessary, and the capacitive output ensures input/output compatibility without a need for level shifting.

There are no shunt capacitances appearing across the TELD in this configuration. The only fringe capacitance that appears across TELD is due to whatever little ohmic contact metallization there is at the anode and cathode. The associated time constant is about 3-4 ps. As the time constant is far less than the domain formation time, memory action will not be present, and single-domain triggering is readily achieved.

The design presented herein is a first-order design. Computer-aided design and simulation must be used to improve these numbers. The objective of simulation will be to maximize subthreshold transconductance, reduce power dissipation, and make it possible to carry out a tolerance analysis and study the effect of fan-in and fan-out.

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Dr. Klaus Mause, FI41 — 1
Forschungsinstitut der DBP beim FTZ
Postfach 800
6100 Darmstadt
Federal Republic of Germany

Prof. Dr. B. G. Bosch — 1
Ruhr-Universitat Bochum
Institut für Elektronik
Postfach 10-21-48
4630 Bochum 1
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